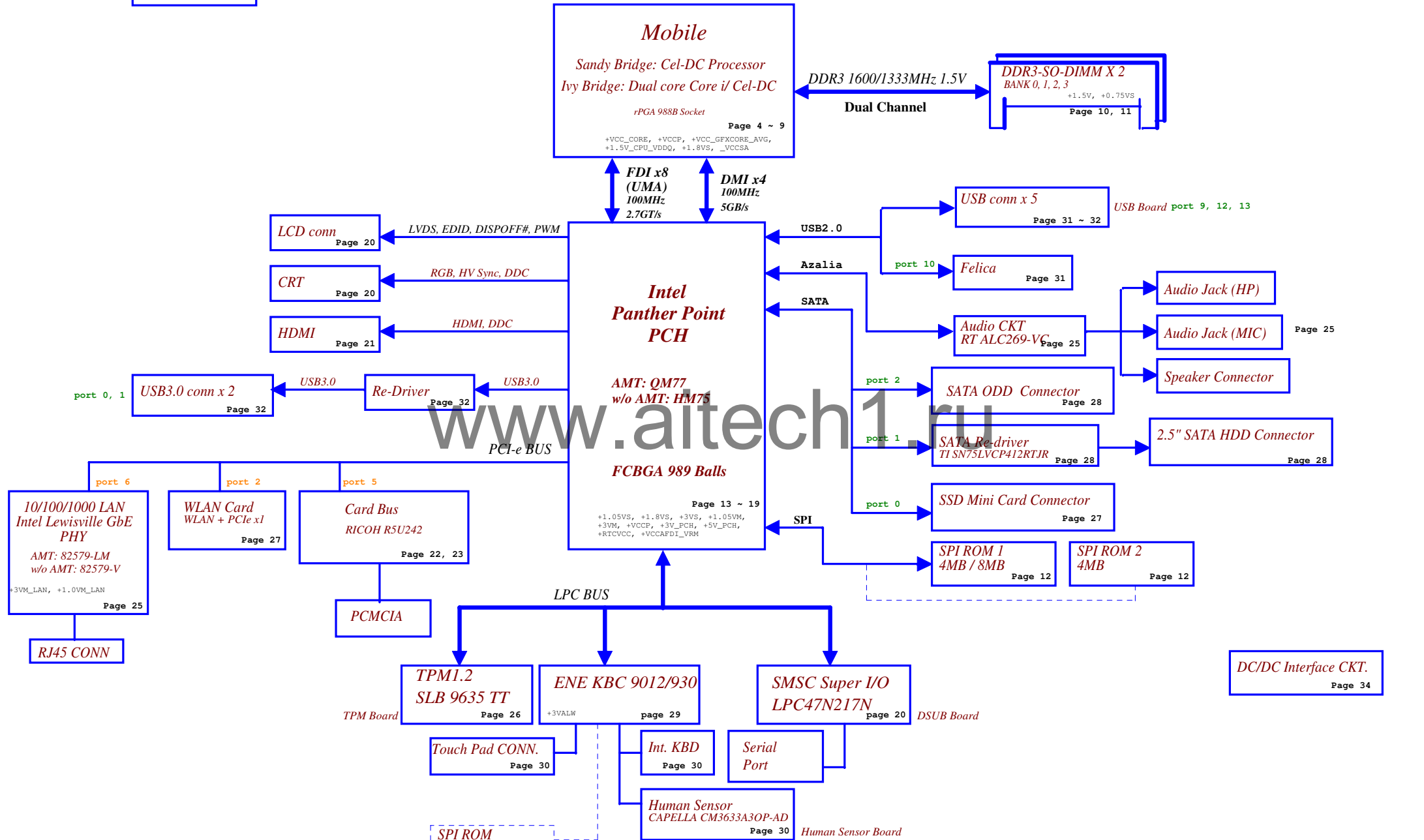


U3CR

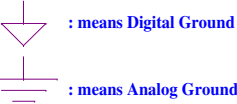
Fan Control  
Page 33



Voltage Rails ( O MEANS ON X MEANS OFF )

<div>power plane</div> <div>State</div>	+RTCVCC	+B +3VL	+5VALW +3VALW	+3V_PCH	+1.05VM_LAN +3VM (SLP_LAN#)	+1.05VM (SLP_A#)	+1.5V +3V	+5VS +3VS +1.5VS +VCC_GFXCORE +VCCP +CPU_CORE +1.8VS +1.05VS +0.75VS +VCCSA
S0	O	O	O	O	O	O	O	O
S3 / DC & no WOL	O	O	O	O	X	X	O	X
S3 / DC & WOL	O	O	O	O	O	X	O	X
S3 / AC & PP1 & no WOL	O	O	O	O	X	X	O	X
S3 / AC & PP1 & WOL	O	O	O	O	O	X	O	X
S3 / AC & PP2 (M3)	O	O	O	O	O	O	O	X
S3 / AC & PP2 (Moff)	O	O	O	O	O	X	O	X
S4 S5 / DC & no WOL	O	O	X	X	X	X	X	X
S4 S5 / DC & WOL	O	O	O	O	O	X	X	X
S4 S5 / AC & PP1 & no WOL	O	O	O	O	X	X	X	X
S4 S5 / AC & PP1 & WOL	O	O	O	O	O	X	X	X
S4 S5 / AC & PP2 (M3)	O	O	O	O	O	O	X	X
S4 S5 / AC & PP2 (Moff)	O	O	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X	X	X

Symbol Note :



Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.10

VD: VD@+USB3@+KB@  
VD: VD@+USB3@+KB@+ROM2@  
VD/10key: VD@+USB3@+10KB@  
VD/10key: VD@+USB3@+10KB@+ROM2@  
VX: VX@+KB@  
VX/10key: VX@+10KB@

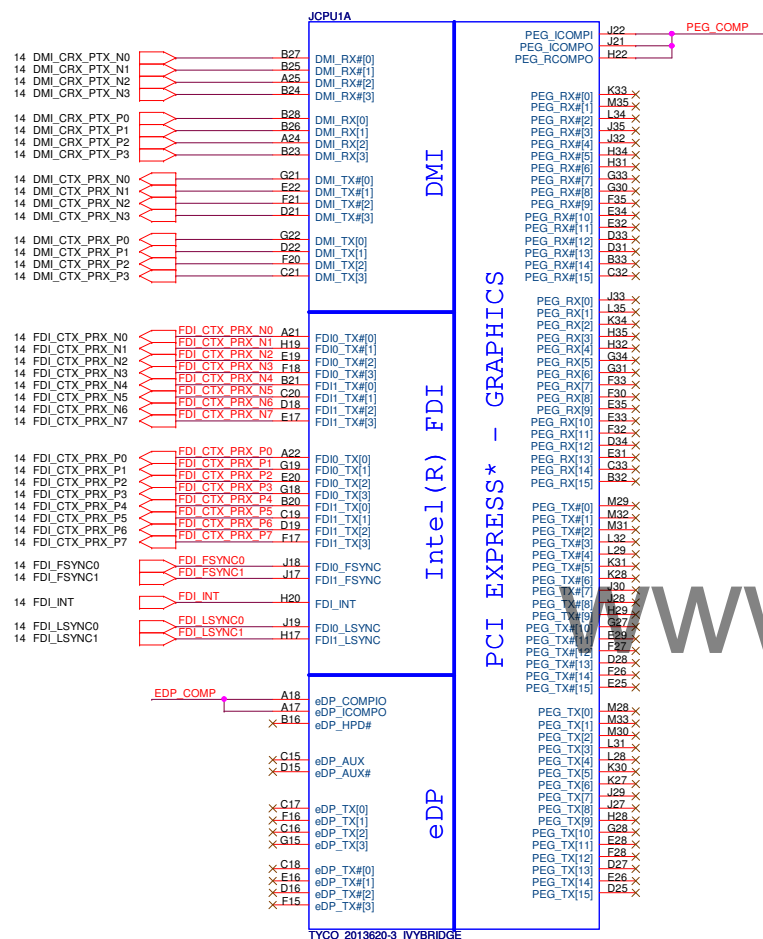
@ : means just reserve , no build  
CONN@ : means ME part.

SMBUS Control Table

	SOURCE	BATT	Charger	Human Sensor	PCH	SODIMM	LAN CHIP	EC-KB930 /EC-KB9012
SMB_EC_CK1 SMB_EC_DA1	EC	V	V	V	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	EC	X	X	X	V	X	X	X
SMBCLK SMBDATA	PCH	X	X	X	X	V	X	X
SML0CLK SML0DATA	PCH	X	X	X	X	X	V	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	V

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra / Rc	100K +/- 5%				
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	3.3K +/- 5%	0.0908 V	0.1054 V	0.121 V	0x08
2	6.8K +/- 5%	0.1817 V	0.2101 V	0.2422 V	0x10
3	10K +/- 5%	0.2601 V	0.3 V	0.3448 V	0x17
4	15K +/- 5%	0.3746 V	0.4304 V	0.4927 V	0x21
5	20K +/- 5%	0.4974 V	0.55 V	0.6076 V	0x2A
6	47K +/- 5%	0.935V	1.055 V	1.184 V	0x3F
7					



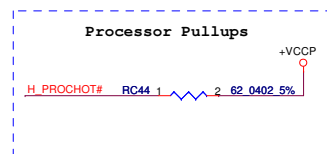
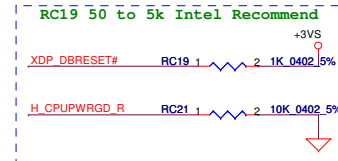
PCI EXPRESS\* - GRAPHICS

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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

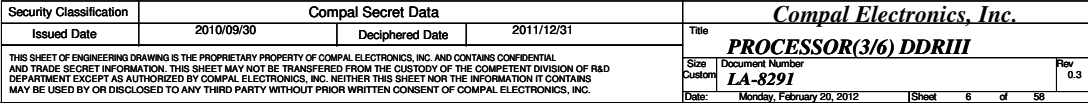
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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Date:	Monday, February 20, 2012	Sheet	4	of	58

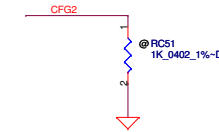


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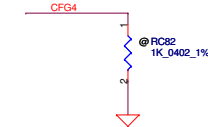




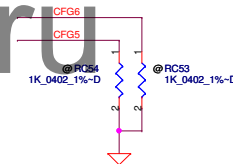
## CFG Straps for Processor



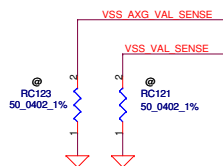
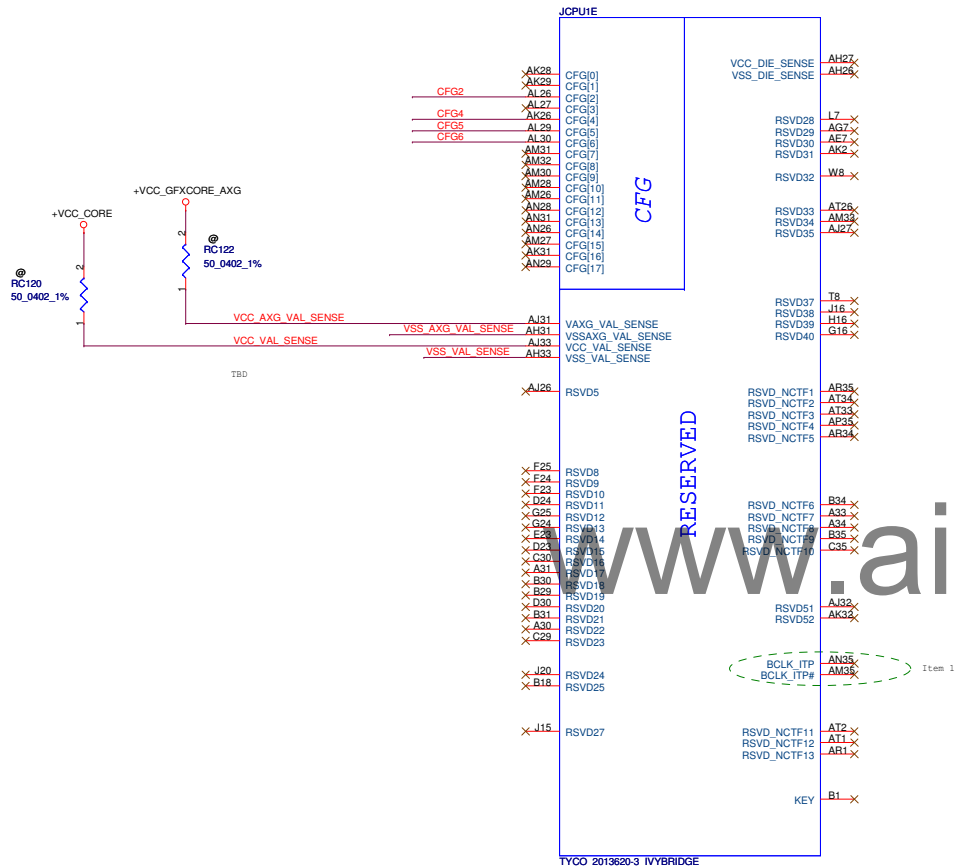
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



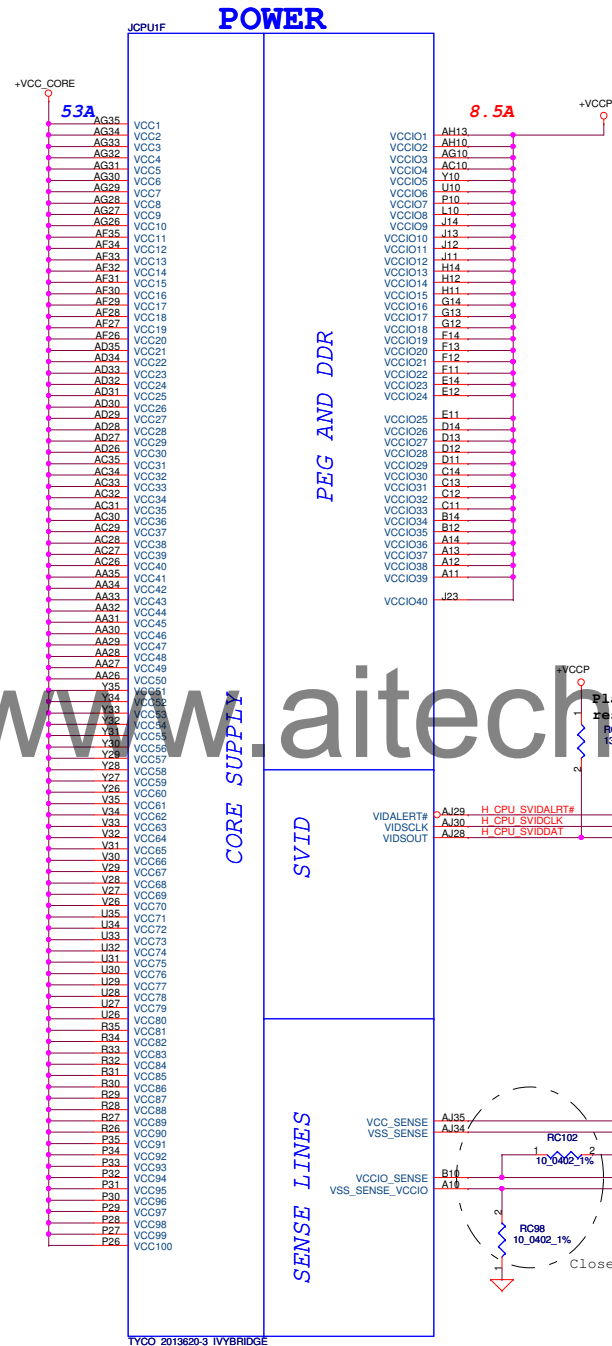
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



INTEL 12/28 recommend  
to add RC120, RC121, RC122, RC123  
Please place as close as JCPU1

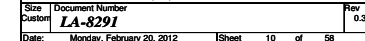
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/30	Deciphered Date	2011/12/31	Title	PROCESSOR(4/6) RSVD,CFG
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				Rev	0.3

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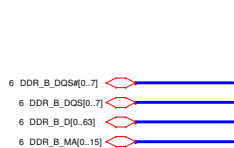


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				Size	Document Number	Rev
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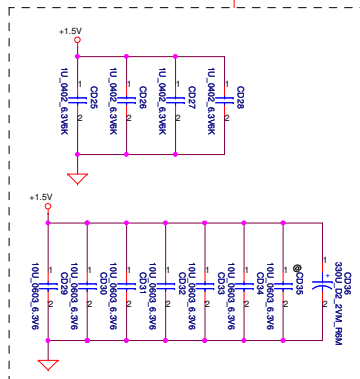
# JDIMMB H=9.2



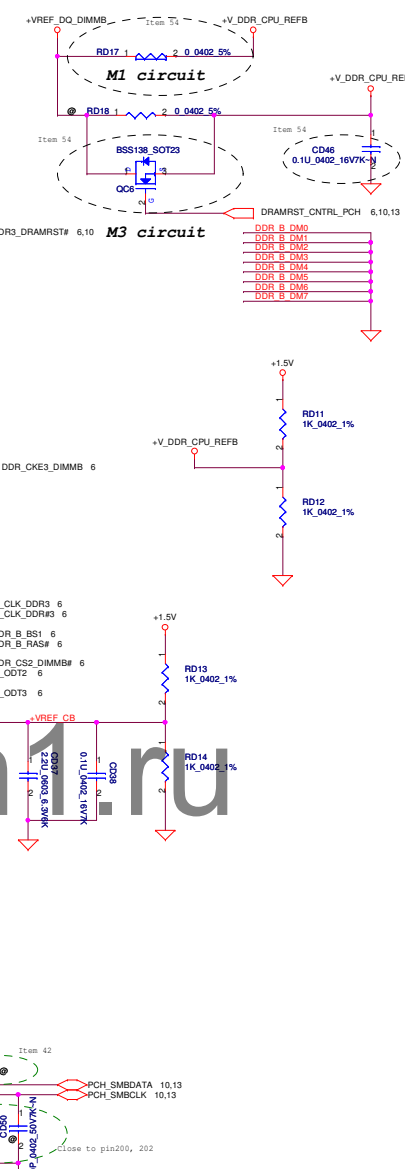
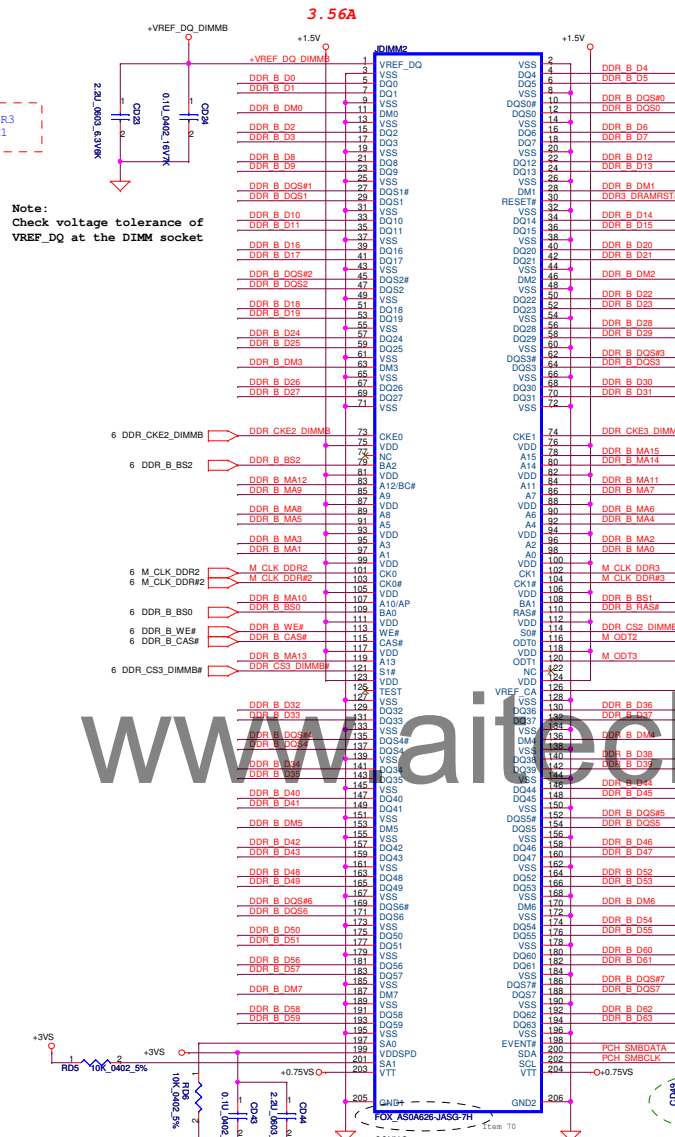
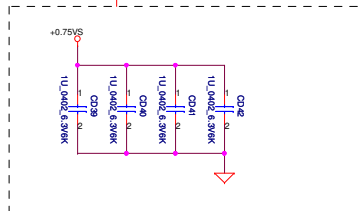
All VREF traces should have 10 mil trace width

Populate R83 for Intel DDR3 VREFDQ multiple methods M1

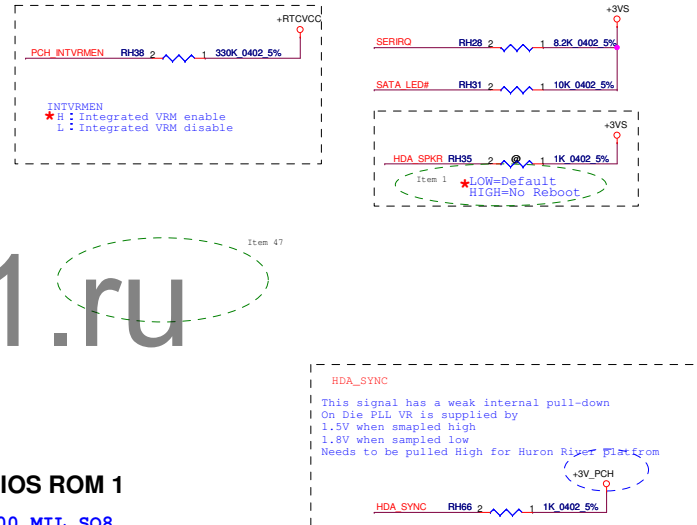
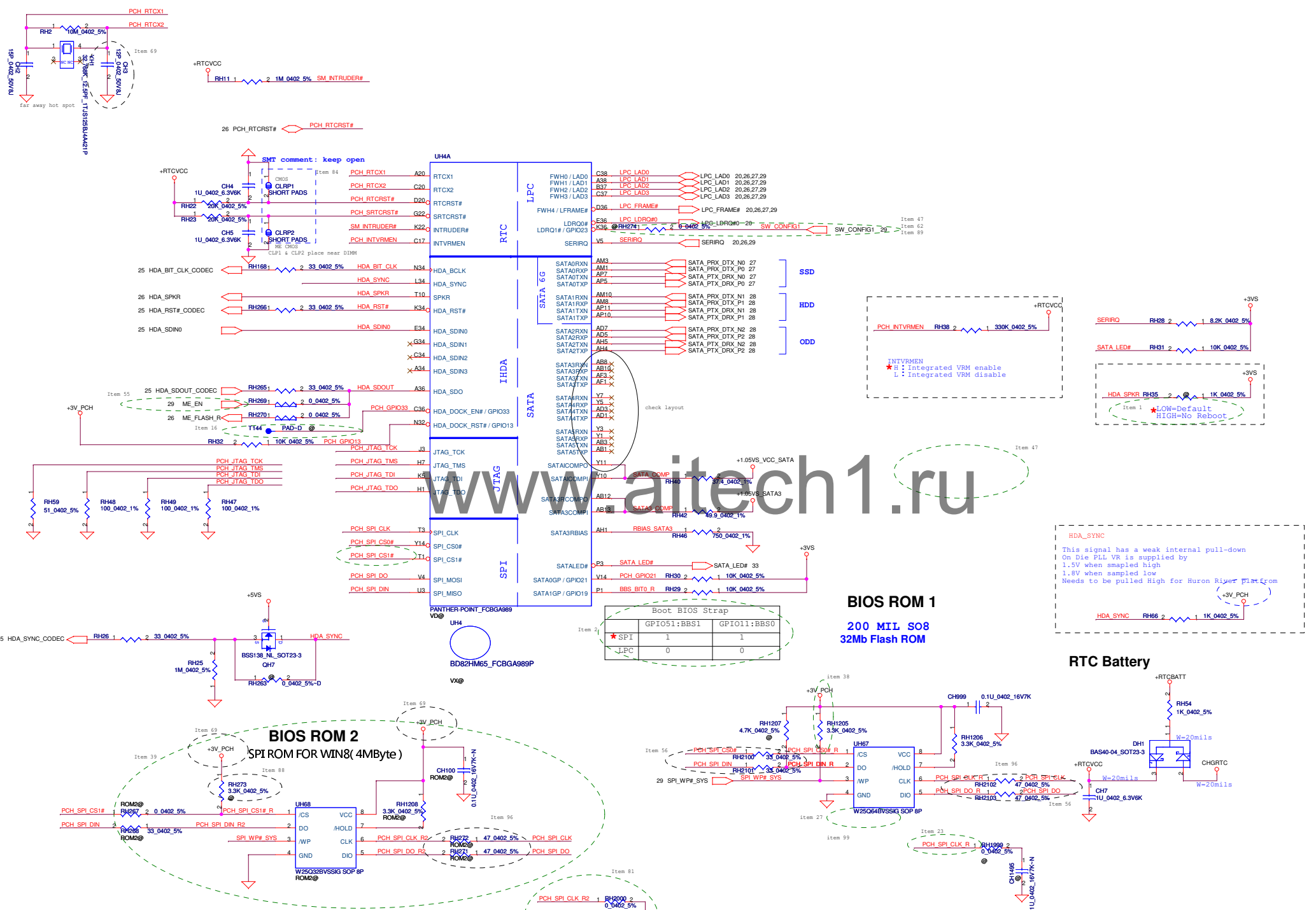
Layout Note: Place near JDIMMB



Layout Note: Place near JDIMMB.203,204



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Boot BIOS Strap			
GPIO51:BBS1		GPIO11:BBS0	
*SPI	1	1	
LPC	0	0	

**BIOS ROM 1**  
200 MIL SO8  
32Mb Flash ROM

**BIOS ROM 2**  
SPI ROM FOR WIN8 (4MByte)

**RTC Battery**



MiniWLAN (Mini Card 1)---->

CARD\_bus ---->

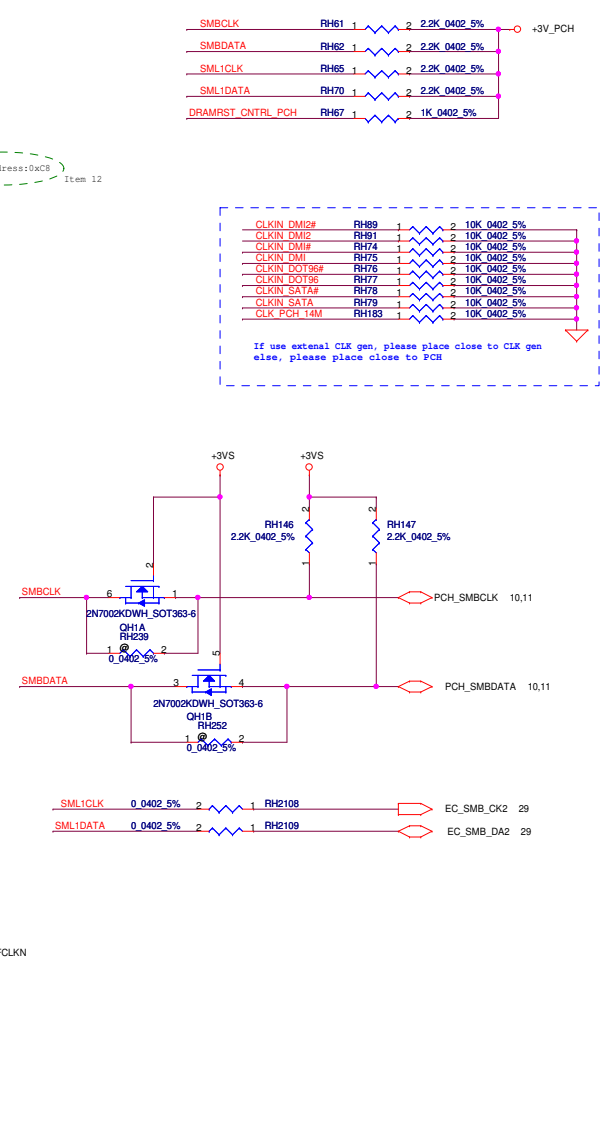
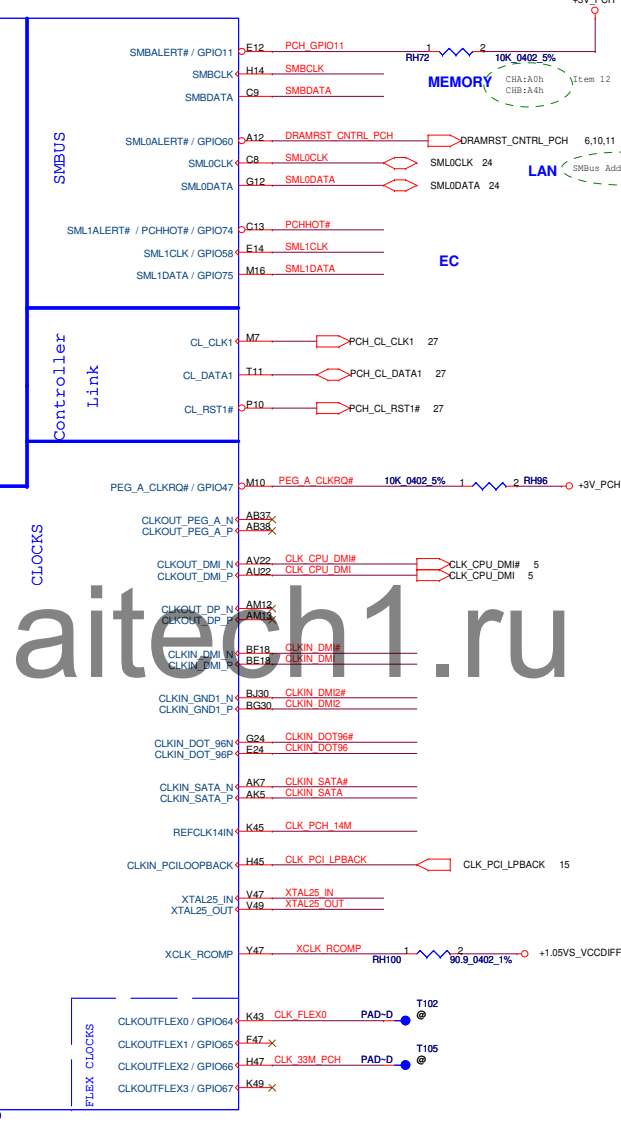
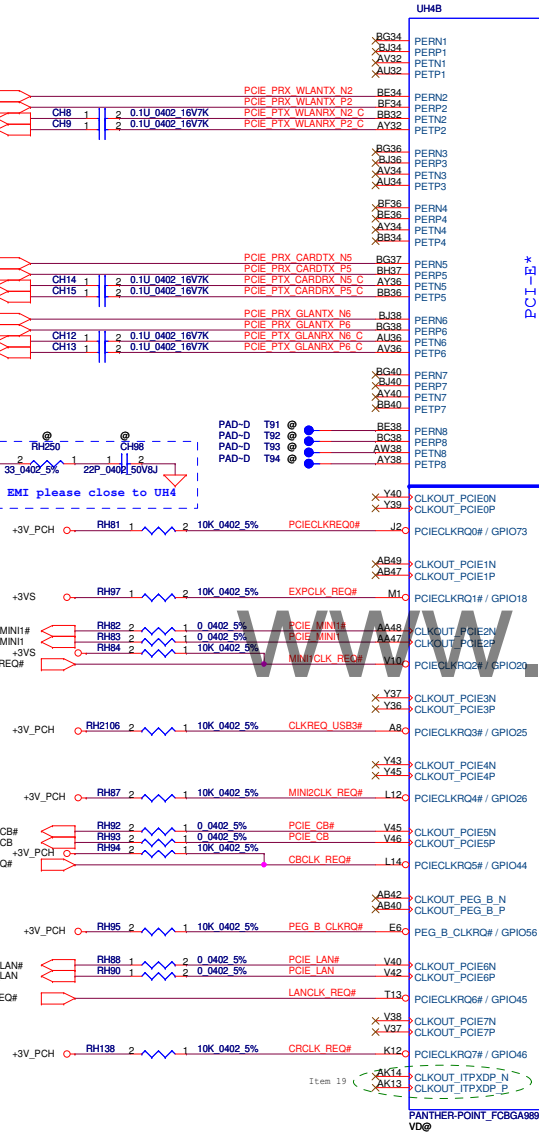
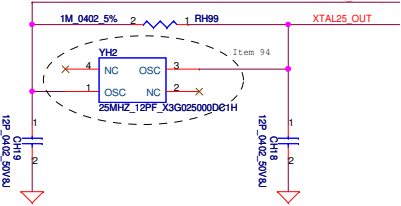
10/100/1G LAN ---->

MiniWLAN (Mini Card 1)---->

MiniWLAN (Mini Card 1)---->

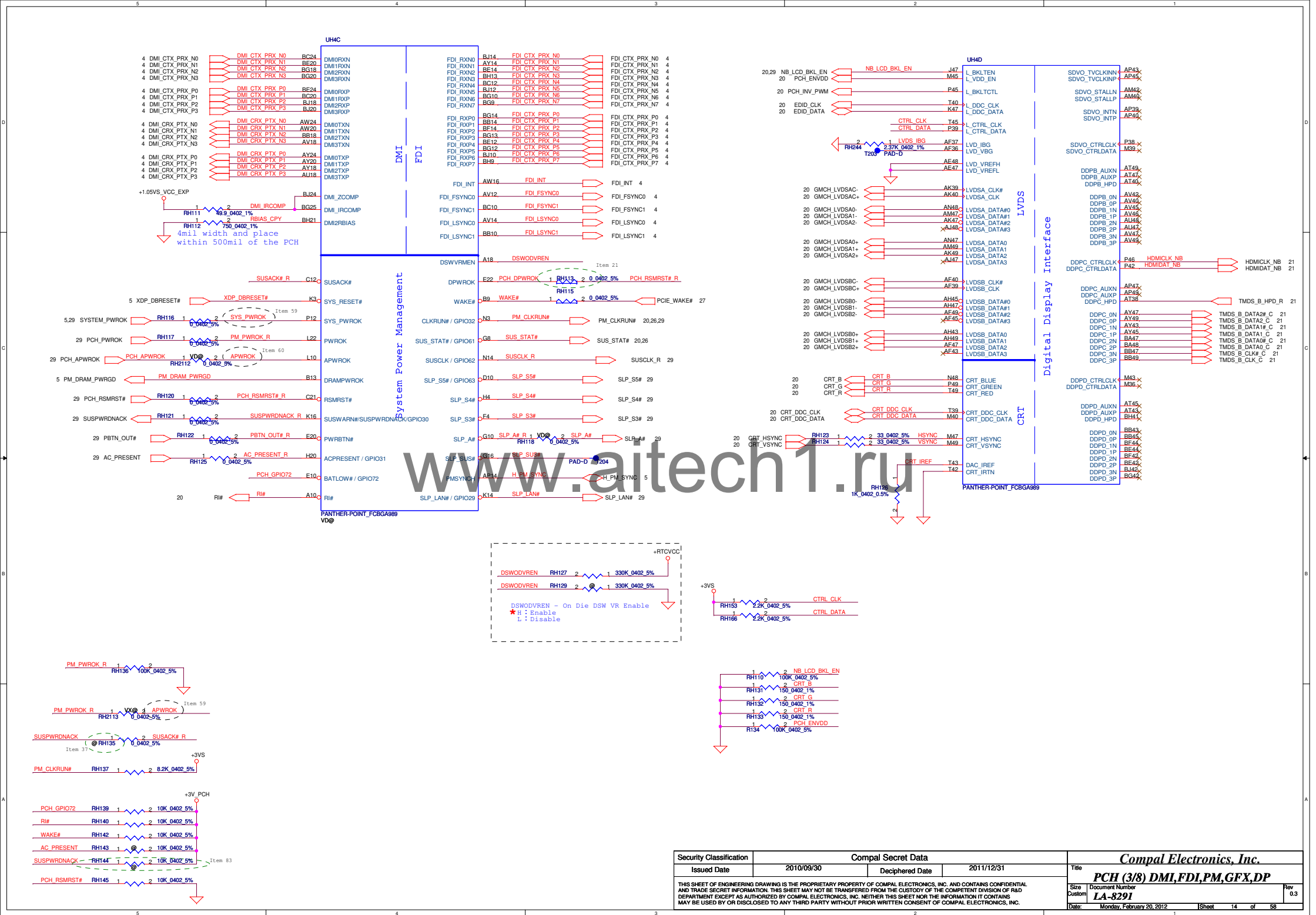
Card BUS ---->

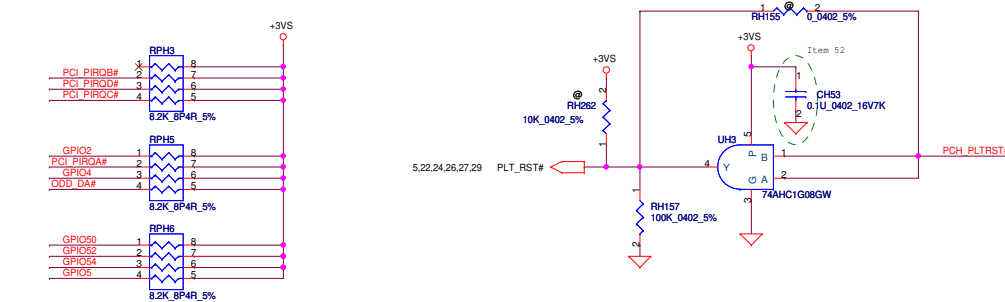
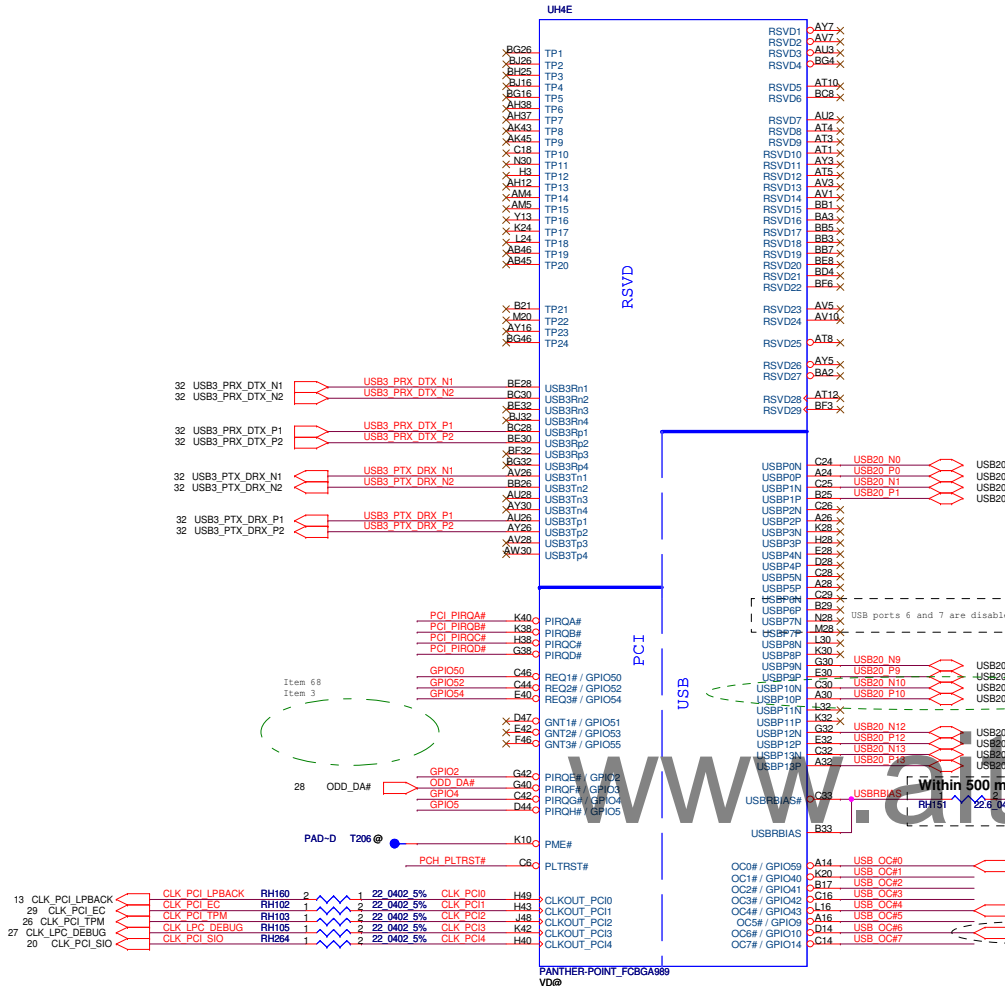
10/100/1G LAN ---->



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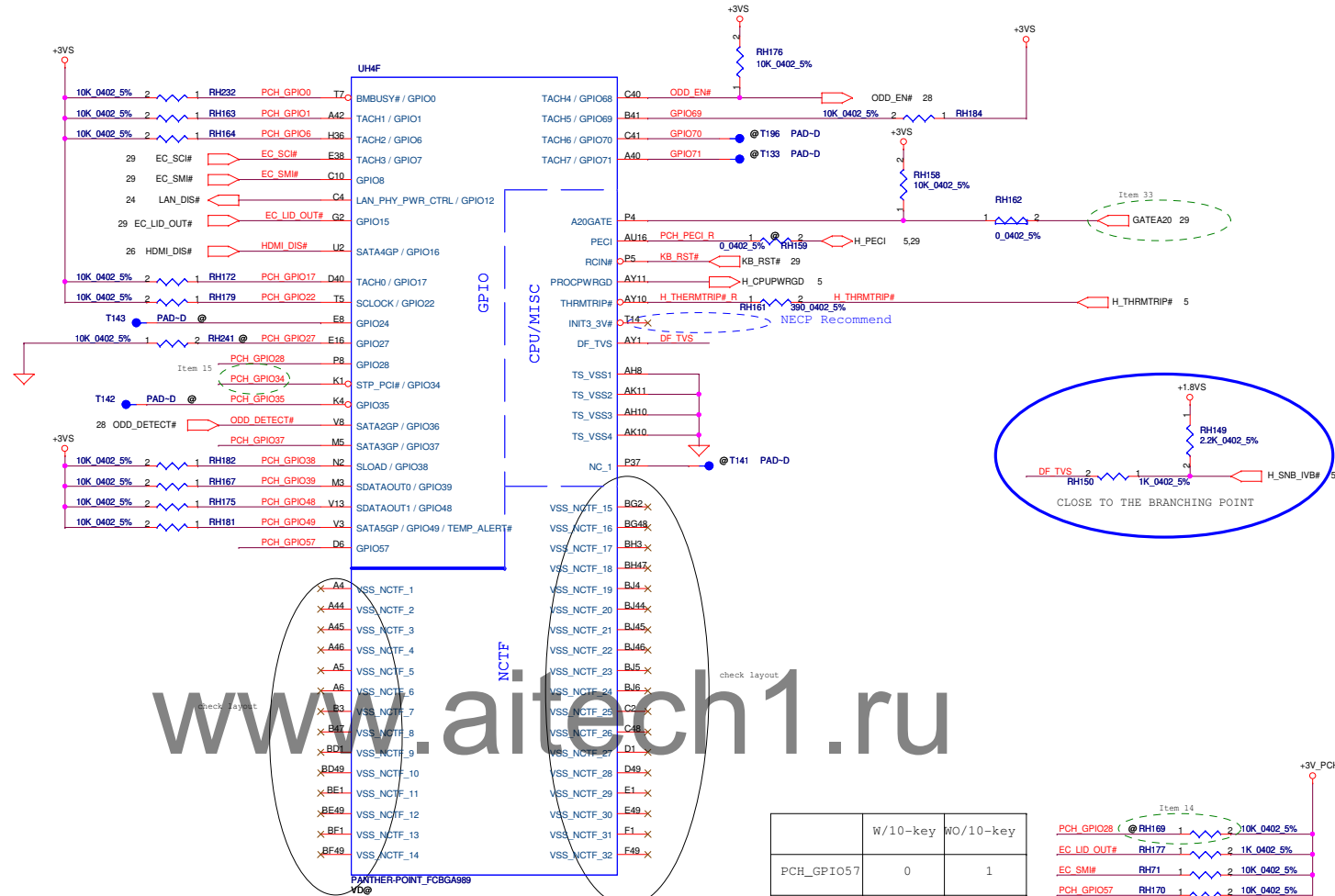




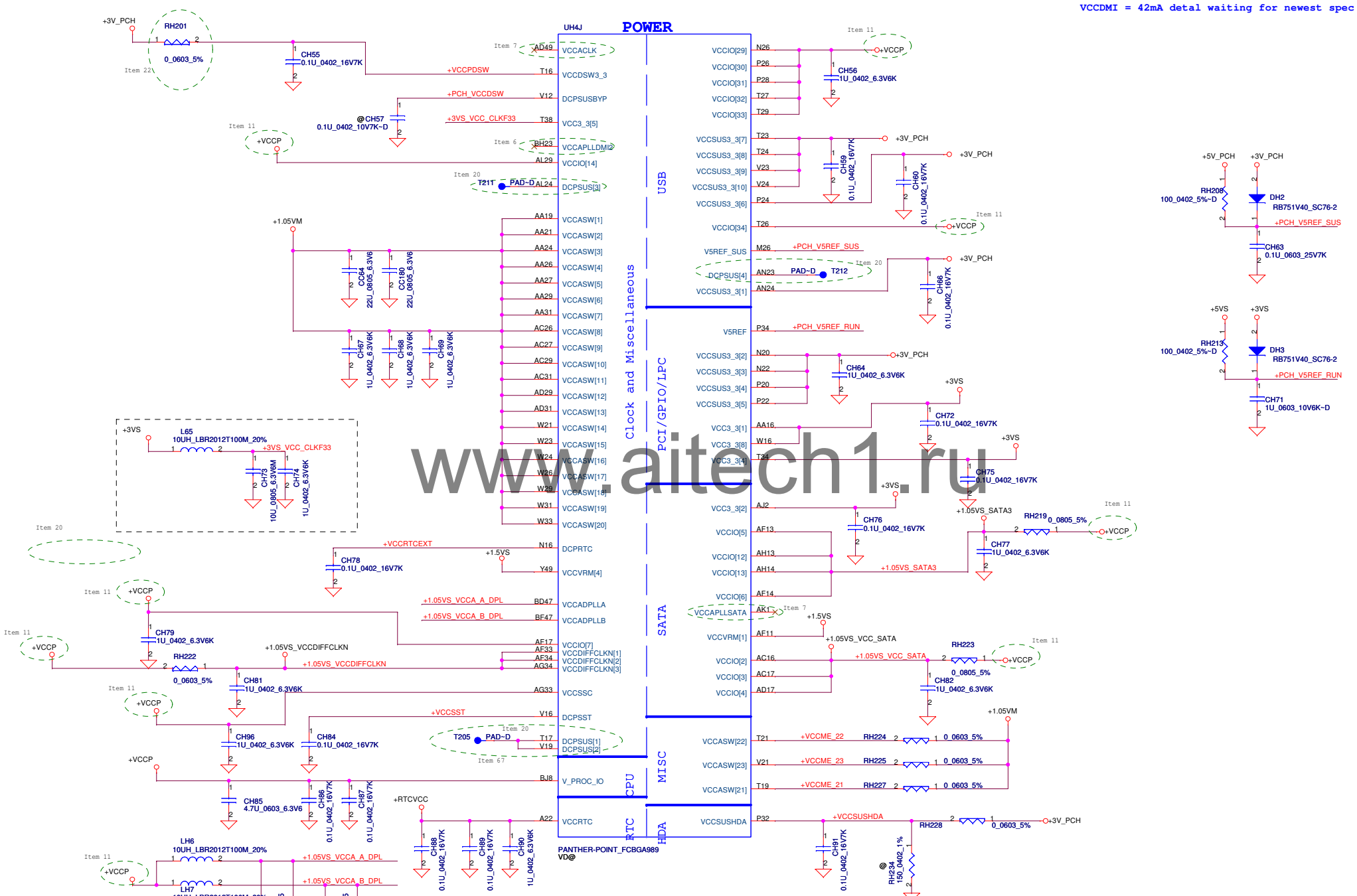
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/30	Deciphered Date	2011/12/31	Title	PCH (4/8) PCI, USB, NVRAM
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U1023  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
\* H: On-Die voltage regulator enable  
L: On-Die PLL Voltage Regulator disable

PCH\_GPIO37  
FDI TERMINATION VOLTAGE OVERRIDE  
\* LOW - Tx, Rx terminated  
to same voltage  
(DC Coupling Mode)



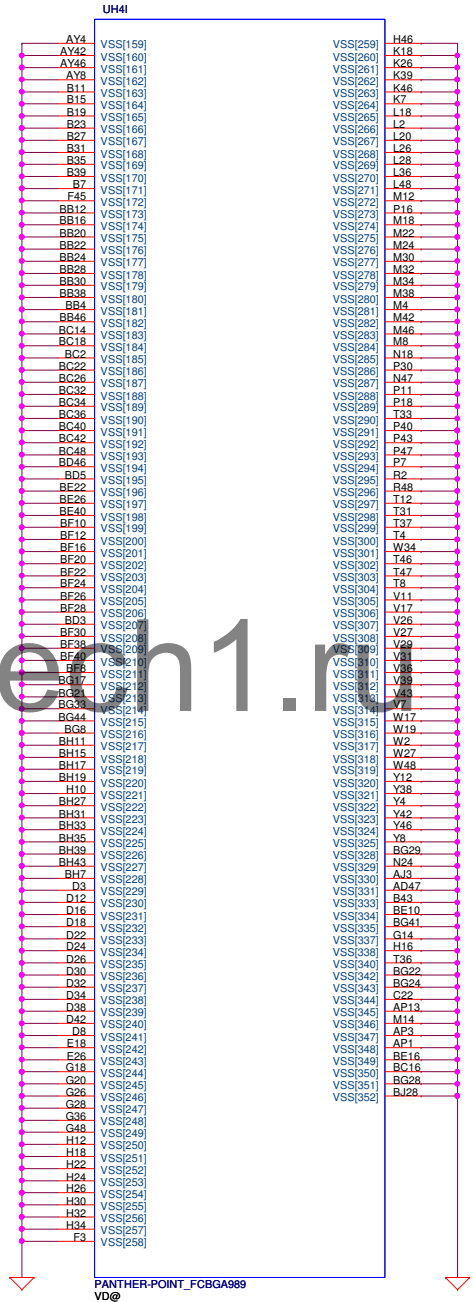
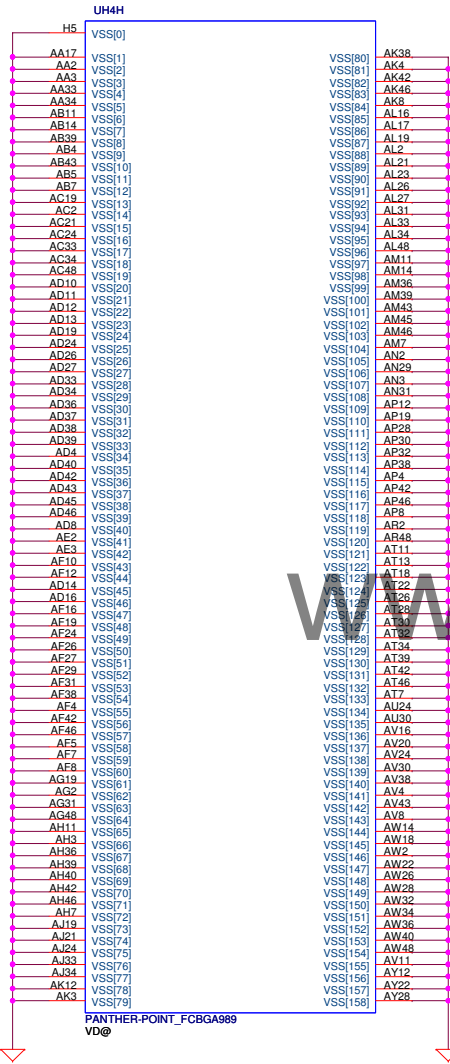



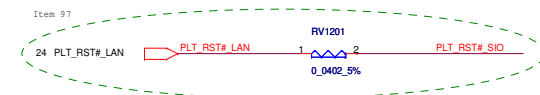
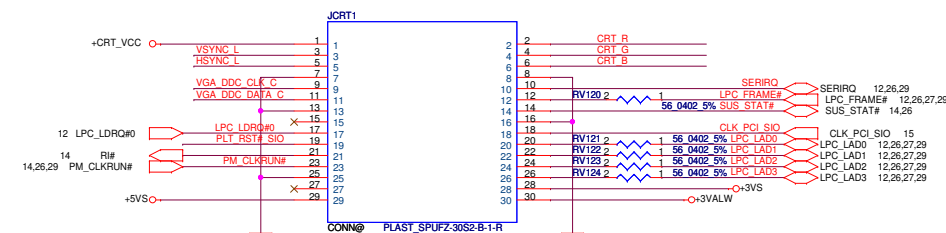


VCC3\_3 = 266mA detal waiting for newest spec  
VCCDMI = 42mA detal waiting for newest spec

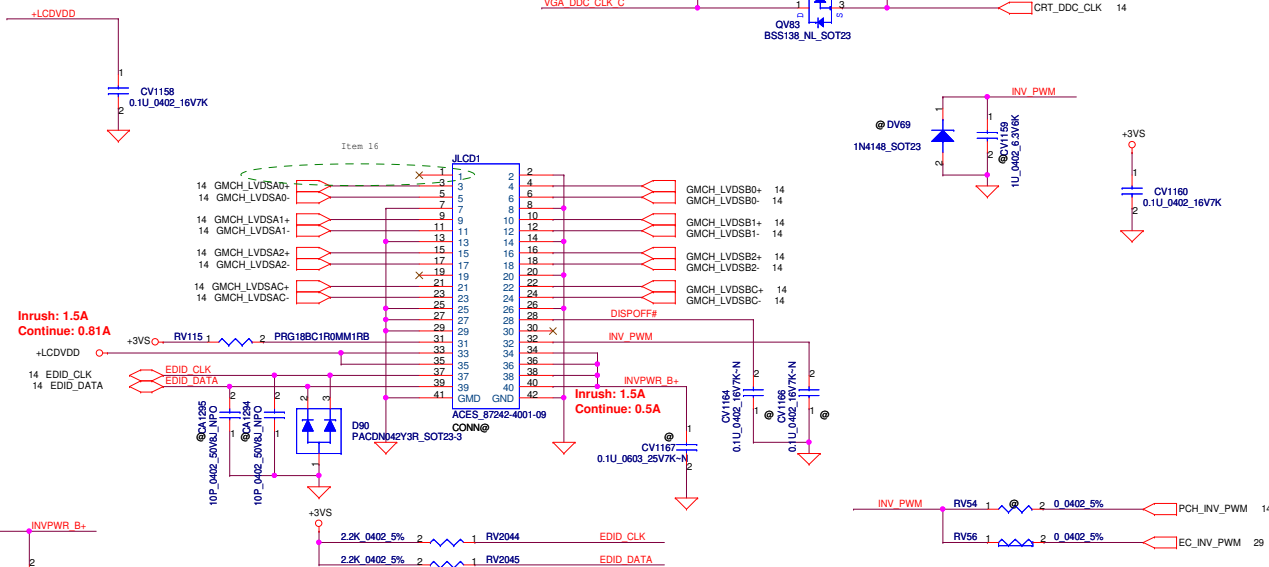
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				PCH (7/8) PWR					
				Size		Document Number		Rev	
				Custom		LA-8291		0.3	
				Date:		Monday, February 20, 2012		Sheet 18 of 58	





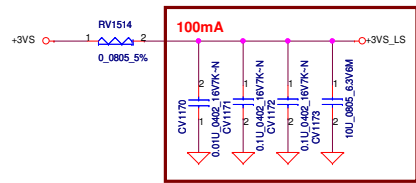
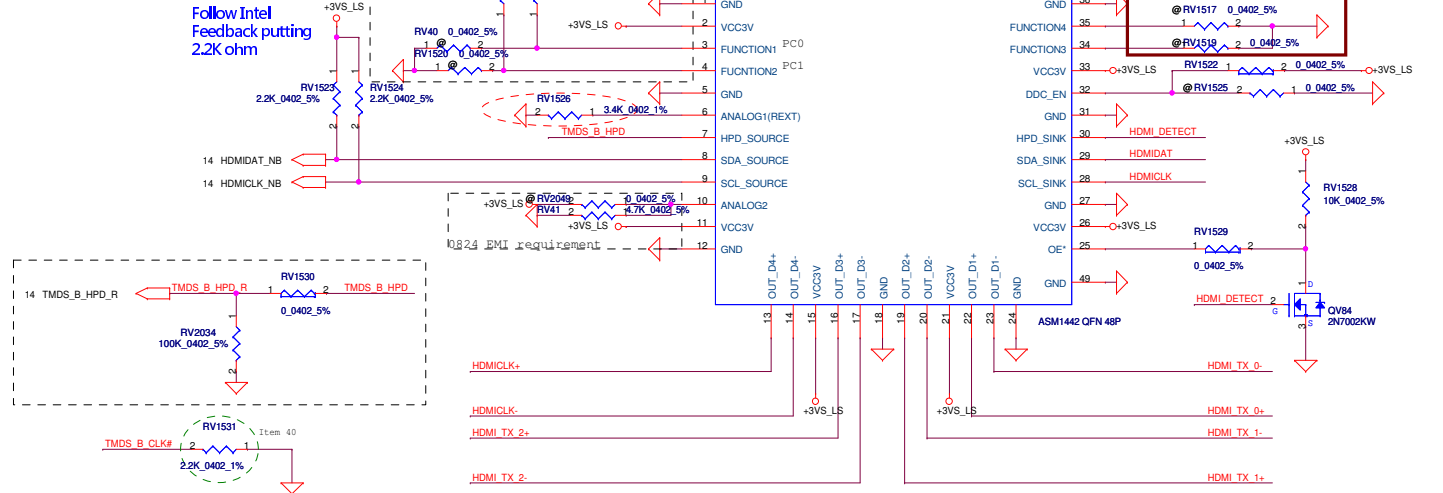
A circuit diagram for component CV1161. It shows a +3VS supply connected to pin 1 of the component. Pin 2 is connected to ground. A capacitor labeled CV1161 with value 1U\_0603\_10V5K is connected between pins 1 and 2. The component is represented by a rectangle with pins 1 and 2 labeled.



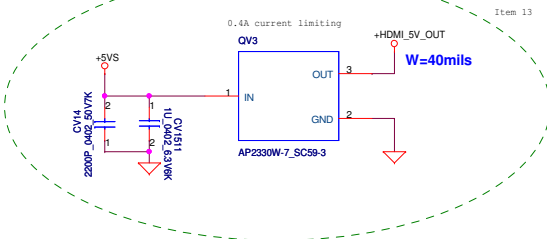
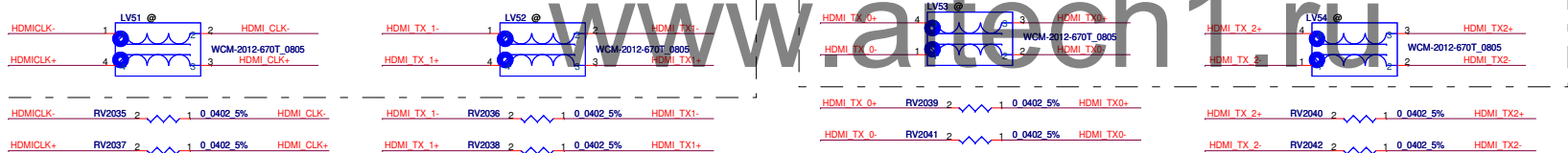
Title	<b><i>CRT CONN/LCD CONN</i></b>
-------	---------------------------------



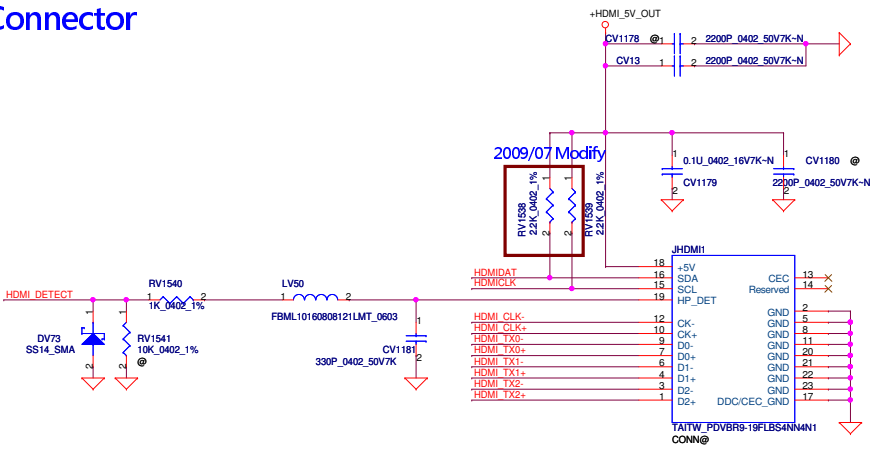
EQUALIZATION SETTING:  
[PC1,PC0]=00,8dB  
[PC1,PC0]=01,4dB (Recommended)  
[PC1,PC0]=10,12dB  
[PC1,PC0]=11,0dB



Co-lay for EMI



## HDMI Connector

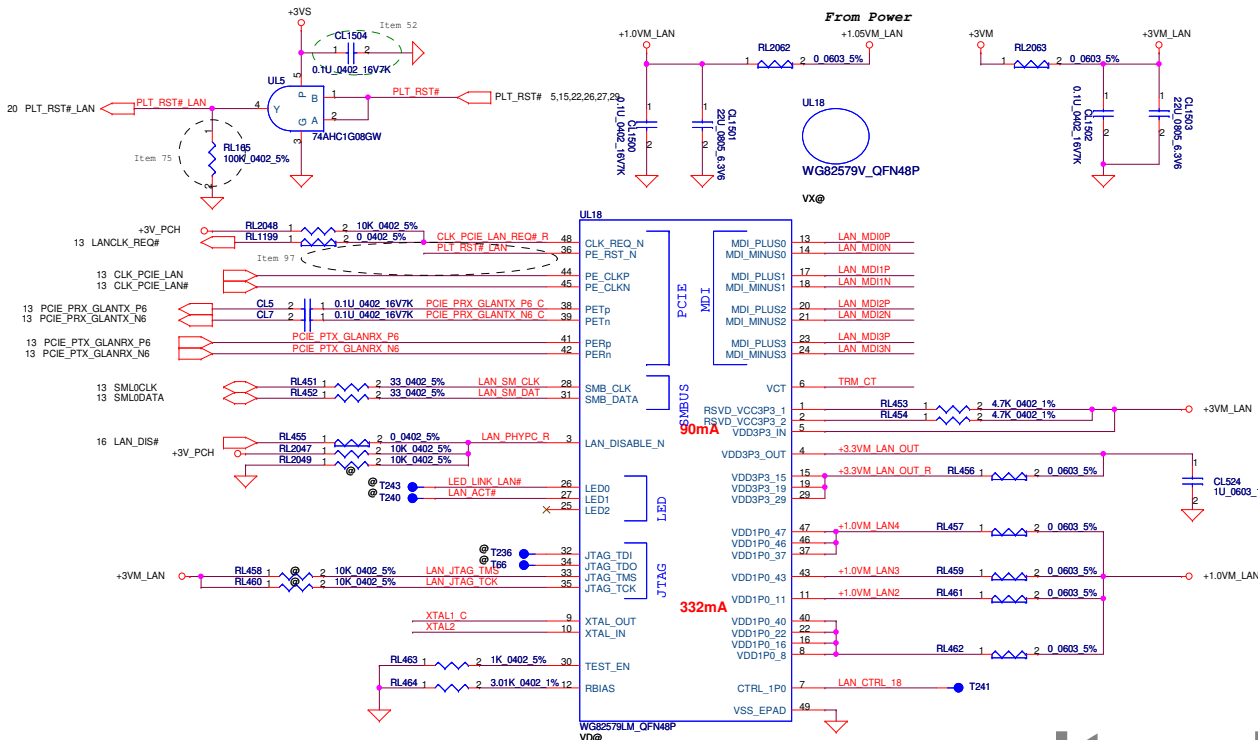


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		LA-8291	Rev 0.3
		Date	Monday, February 20, 2012
		Sheet	21 of 58

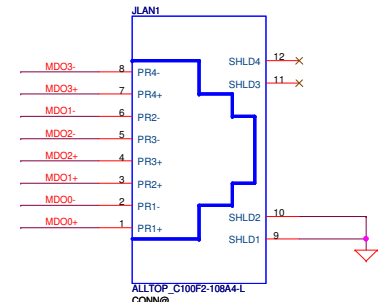




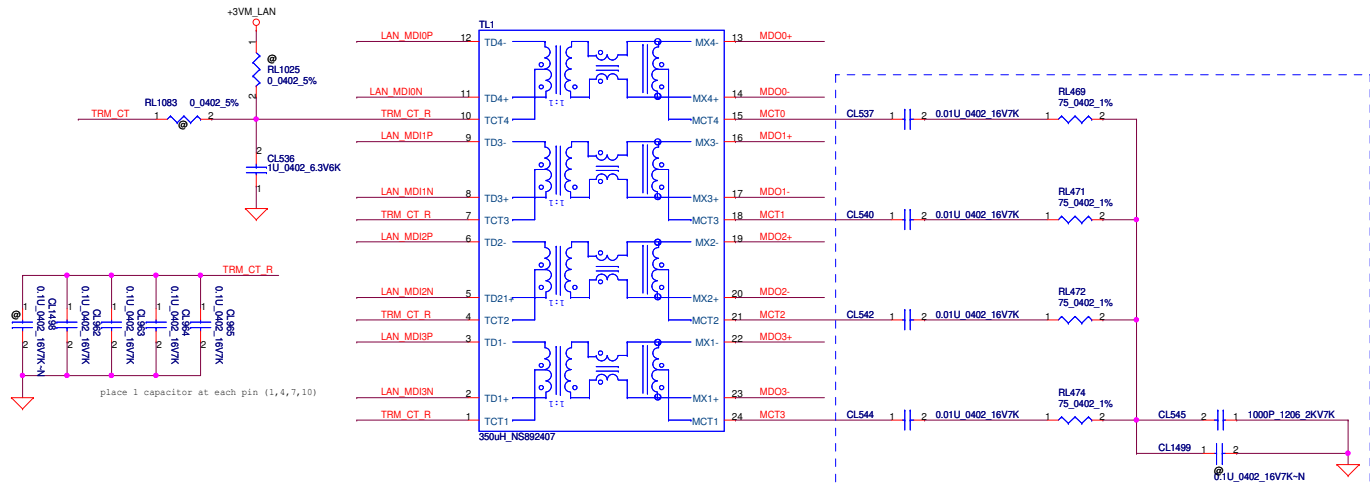


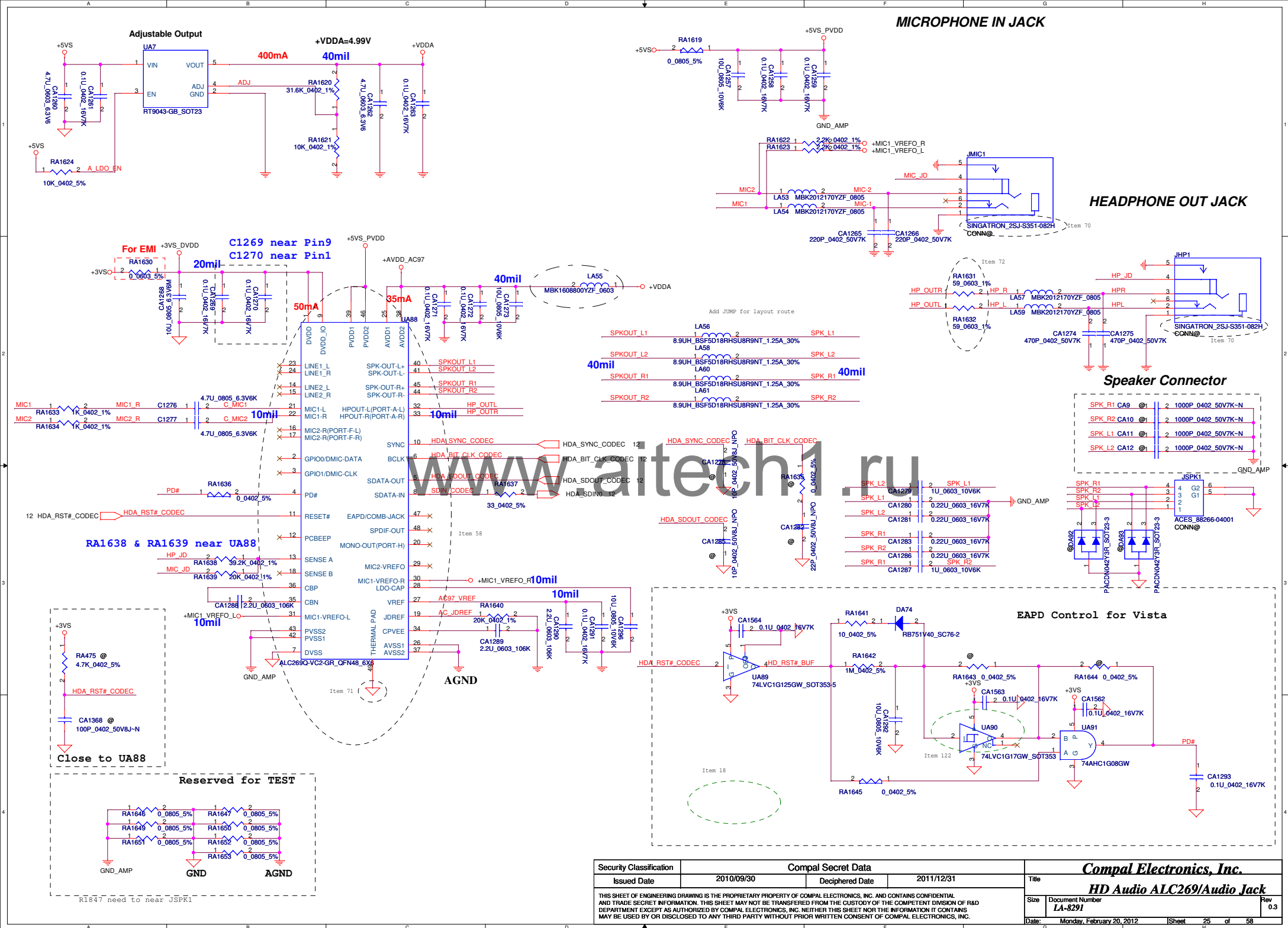


RJ-45 CONN.



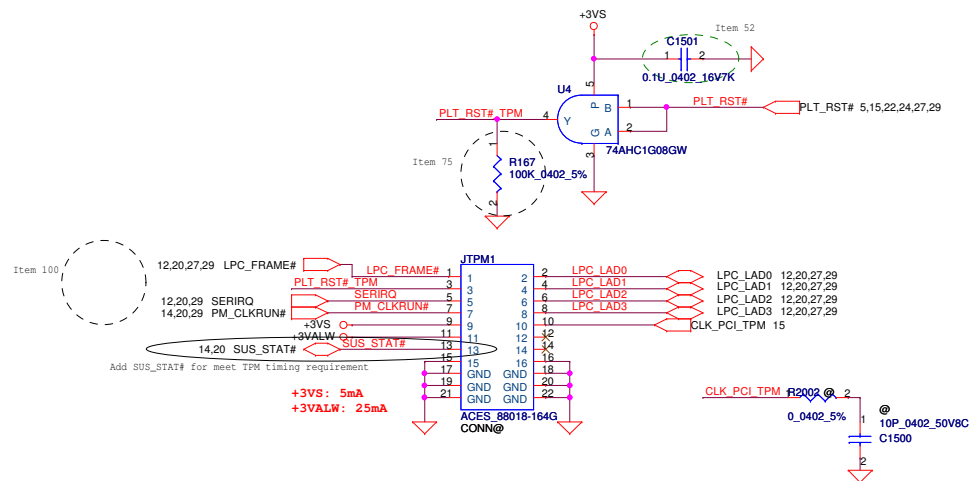
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				Document Number <b>1A-8291</b>	0.3
Date: Monday, February 20, 2012				Sheet	25 of 58

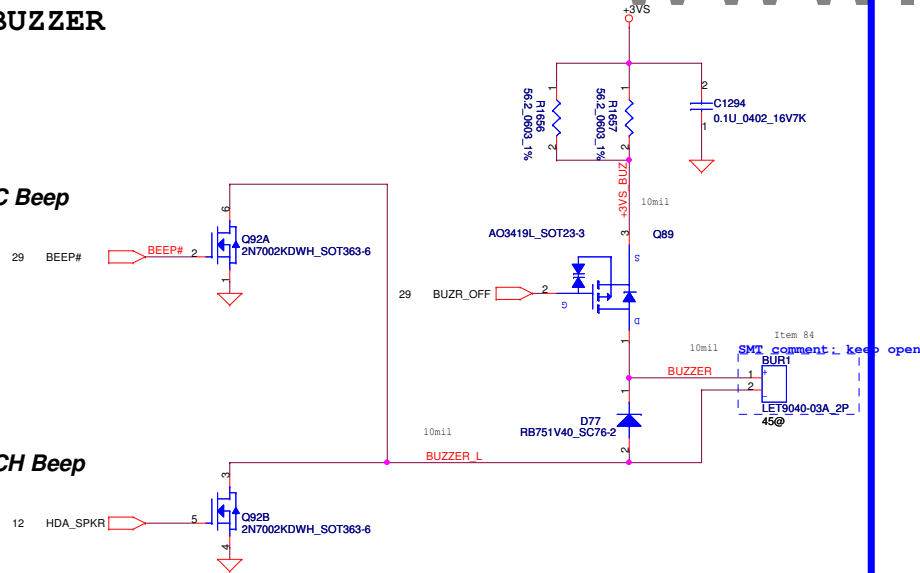
TPM 1.2 Conn



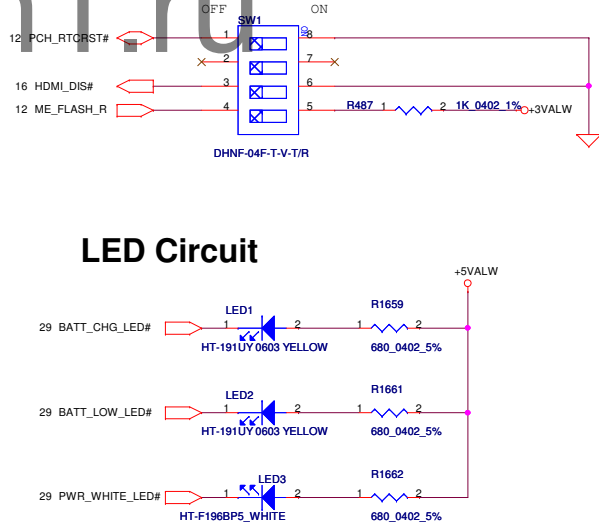
BUZZER

EC Beep

PCH Beep

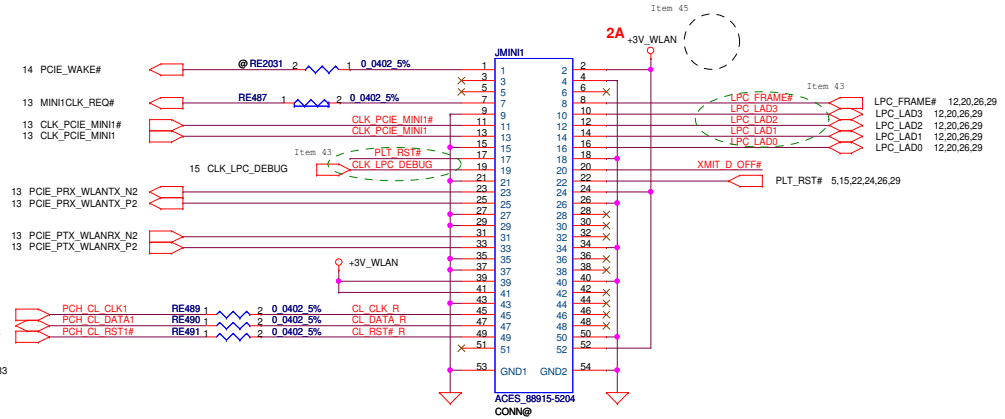
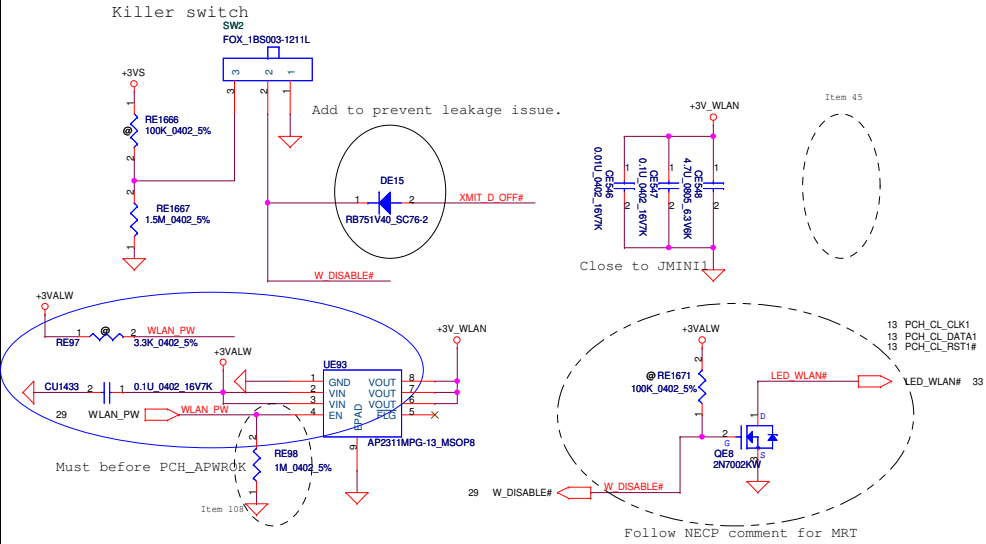


LED Circuit

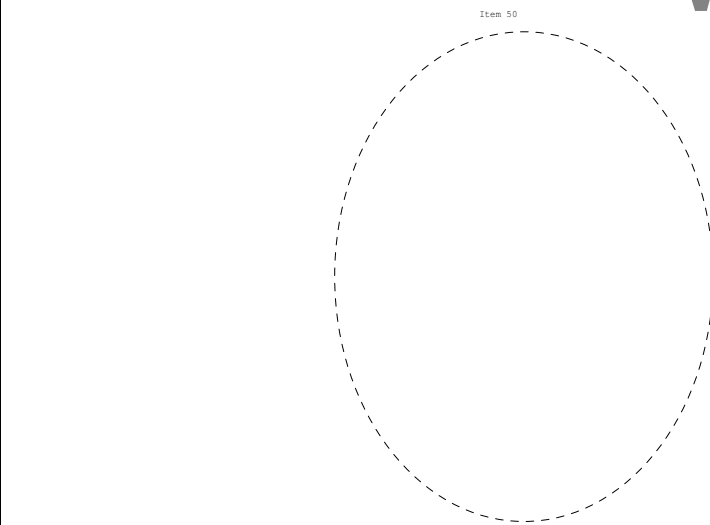


## WLAN (Mini Card1)

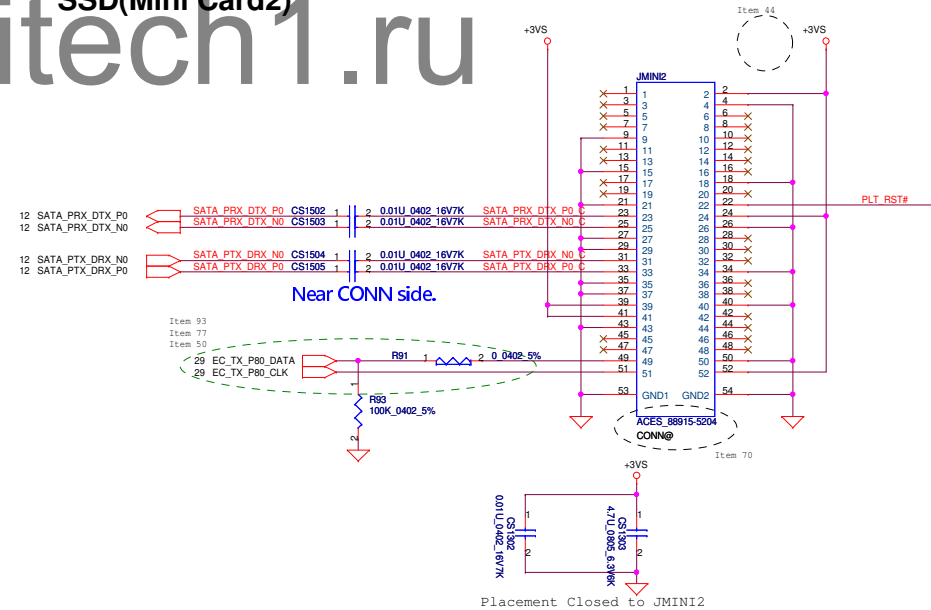
Reserve for port80 card use for FCS in factory side.



## 80 Port(Debug Card)

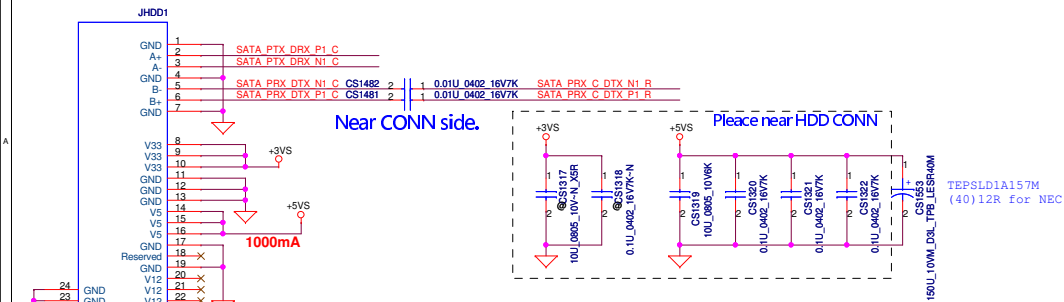


## SSD(Mini Card2)

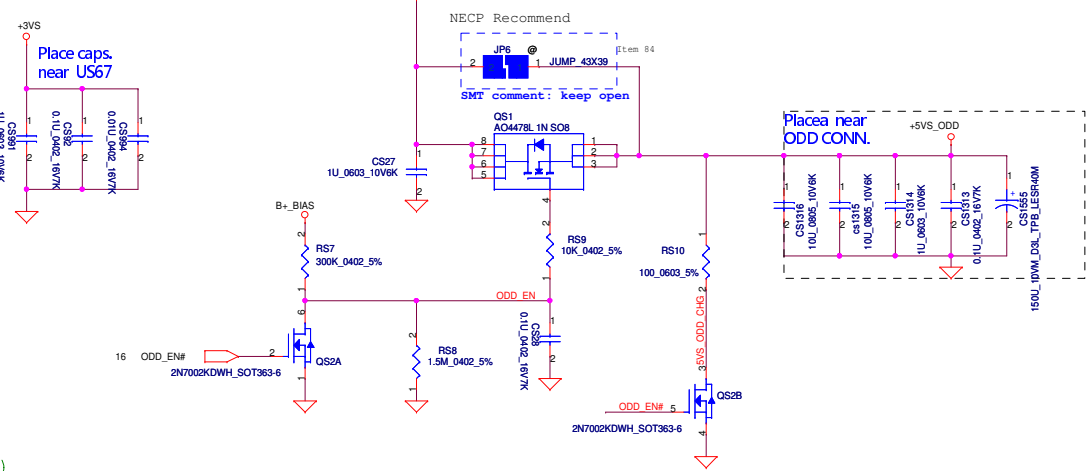
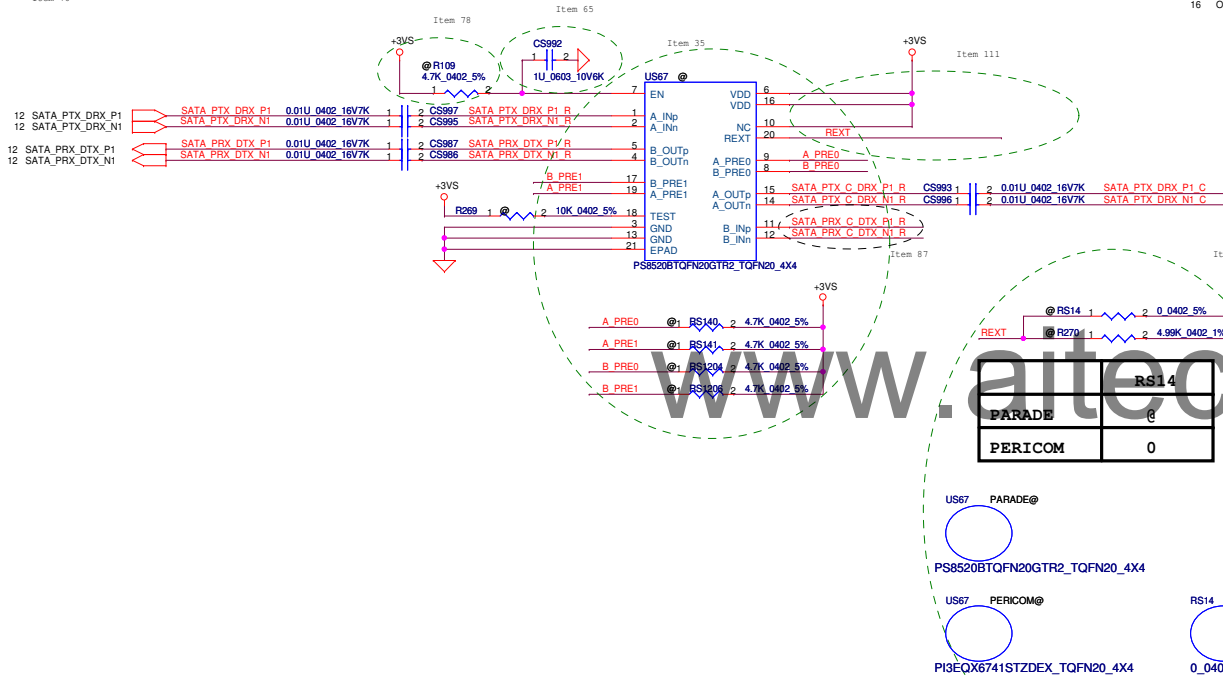


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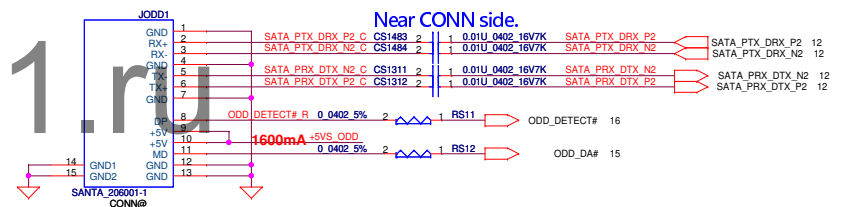
# SATA HDD CONN.



## HDD-SATA Redriver



## SATA ODD CONN.

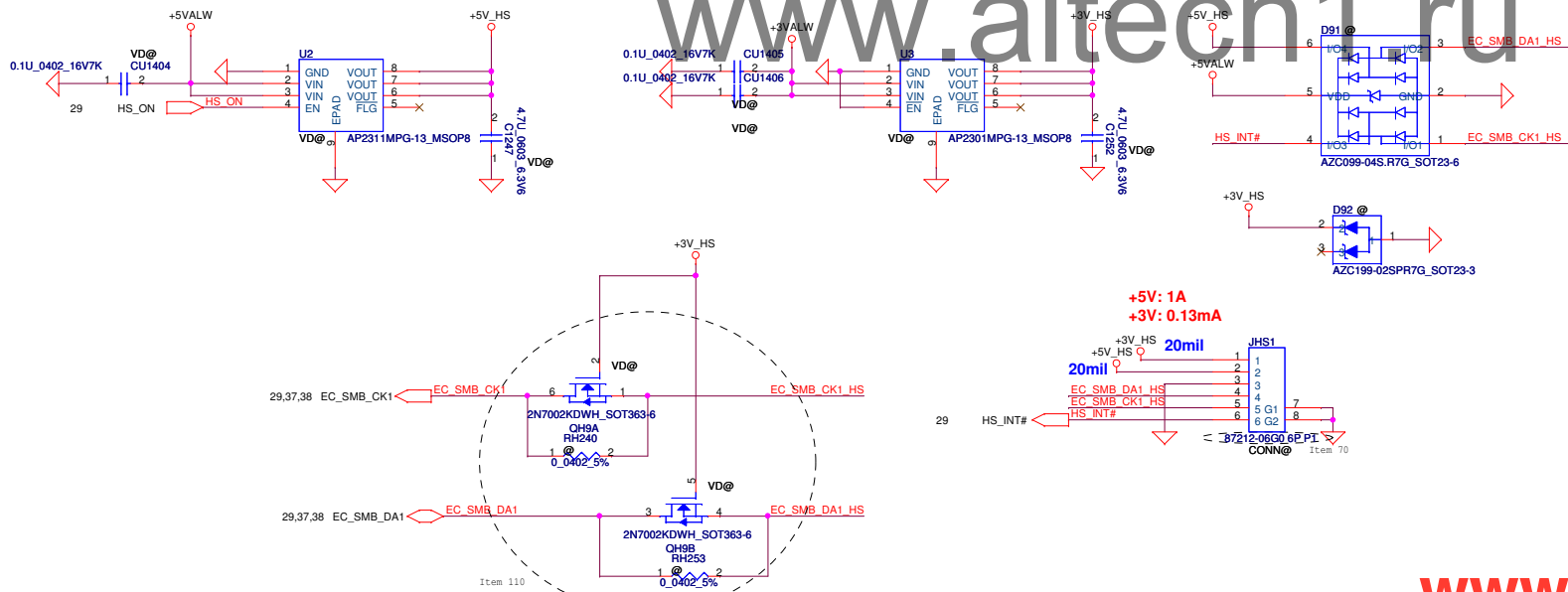
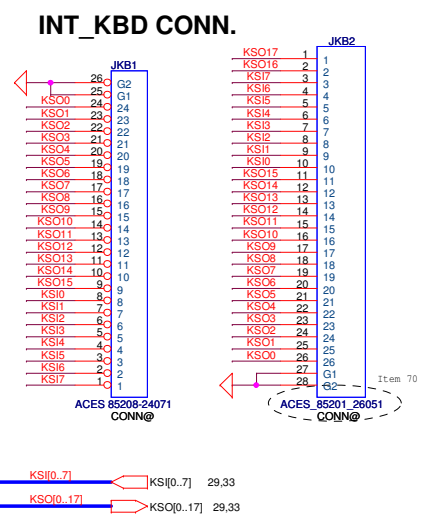
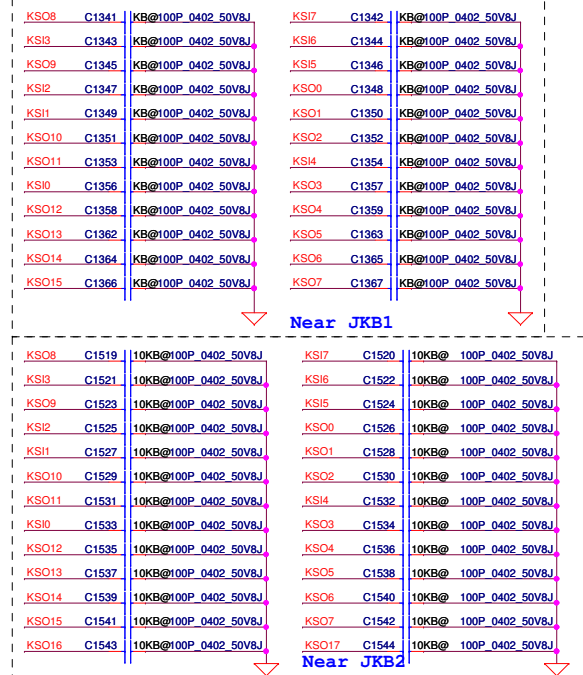
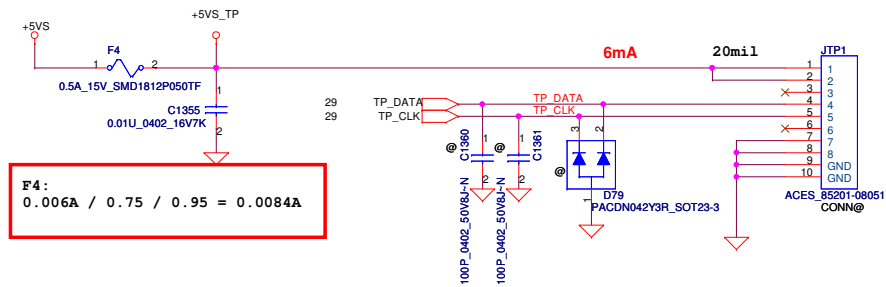






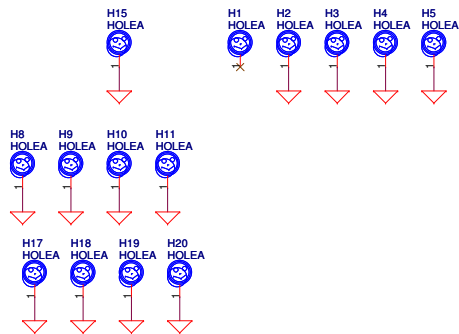
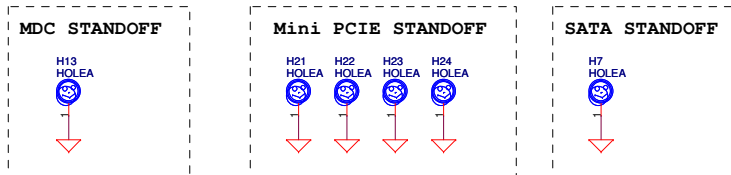


## TouchPad

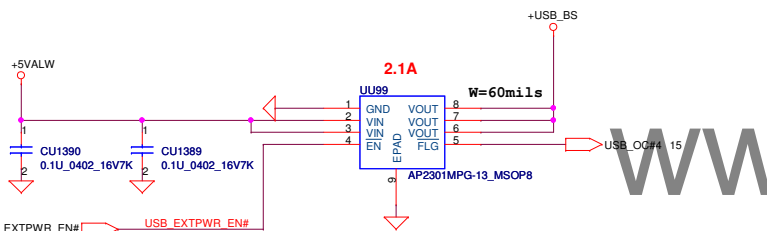


**www.vinafix.vn**

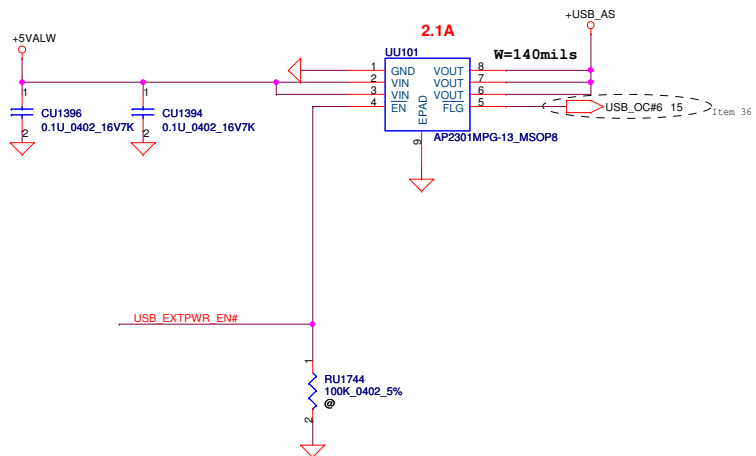
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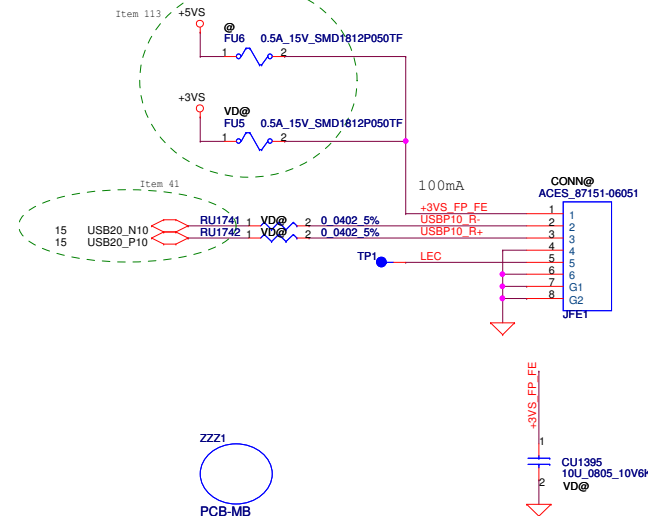


## USB Sub Board CONN.



$$FUS: 0.1A / 0.75 / 0.95 = 0.14A$$

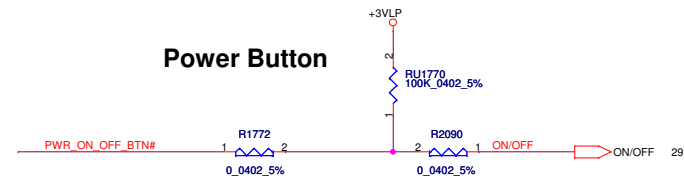
## Felica Conn



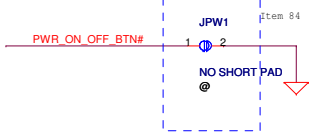
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				Size	Document Number
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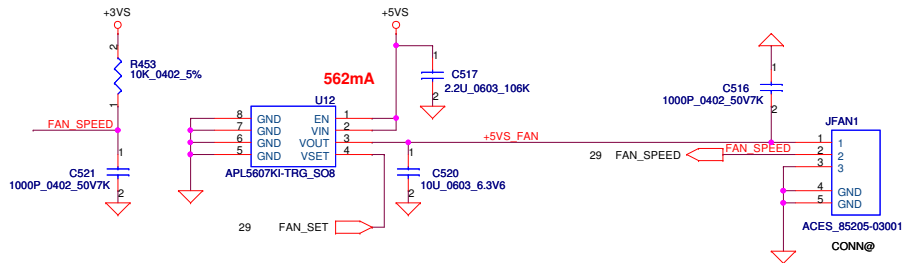
## Power Button



SMT comment: keep open

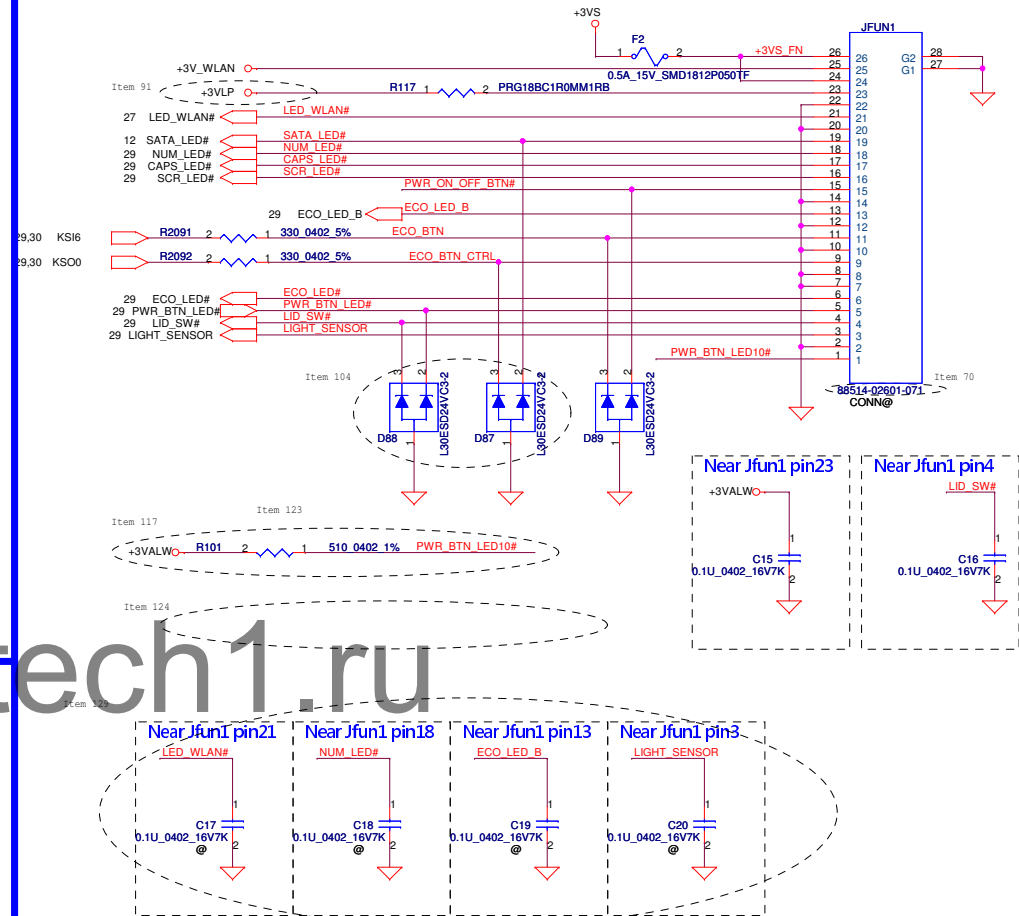


## Fan Control Circuit

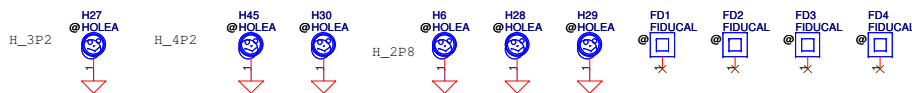


## Function/B CONN.

$$F2: 0.16A / 0.75 / 0.95 = 0.225A$$



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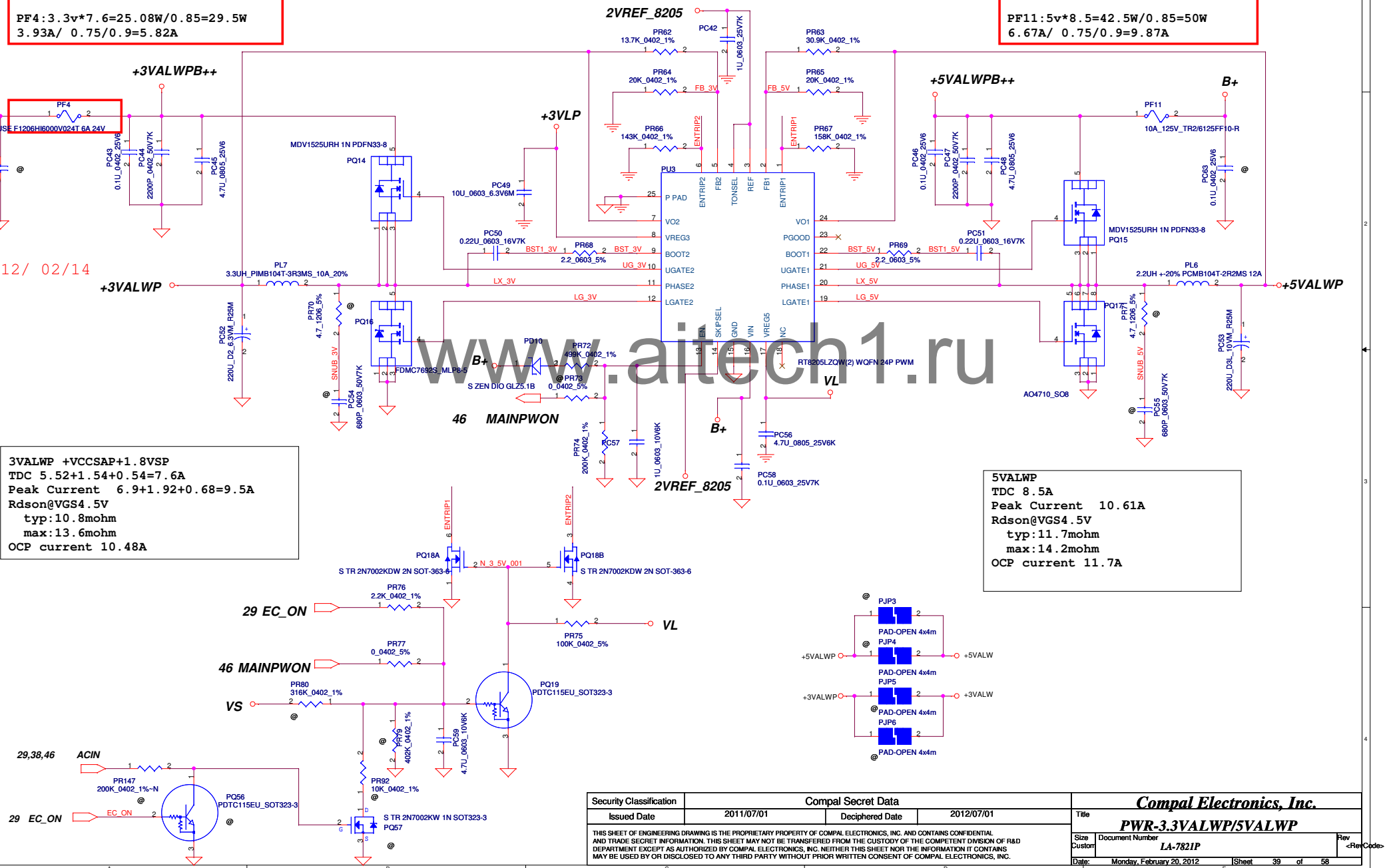
PF4:  $3.3\text{v} \times 7.6 = 25.08\text{W} / 0.85 = 29.5\text{W}$   
 $3.93\text{A} / 0.75 / 0.9 = 5.82\text{A}$

PF11:  $5\text{v} \times 8.5 = 42.5\text{W} / 0.85 = 50\text{W}$   
 $6.67\text{A} / 0.75 / 0.9 = 9.87\text{A}$

12/ 02/14

3VALWP +VCCSAP+1.8VSP  
TDC  $5.52 + 1.54 + 0.54 = 7.6\text{A}$   
Peak Current  $6.9 + 1.92 + 0.68 = 9.5\text{A}$   
Rdson@VGS4.5V  
typ: 10.8mohm  
max: 13.6mohm  
OCP current 10.48A

5VALWP  
TDC 8.5A  
Peak Current 10.61A  
Rdson@VGS4.5V  
typ: 11.7mohm  
max: 14.2mohm  
OCP current 11.7A

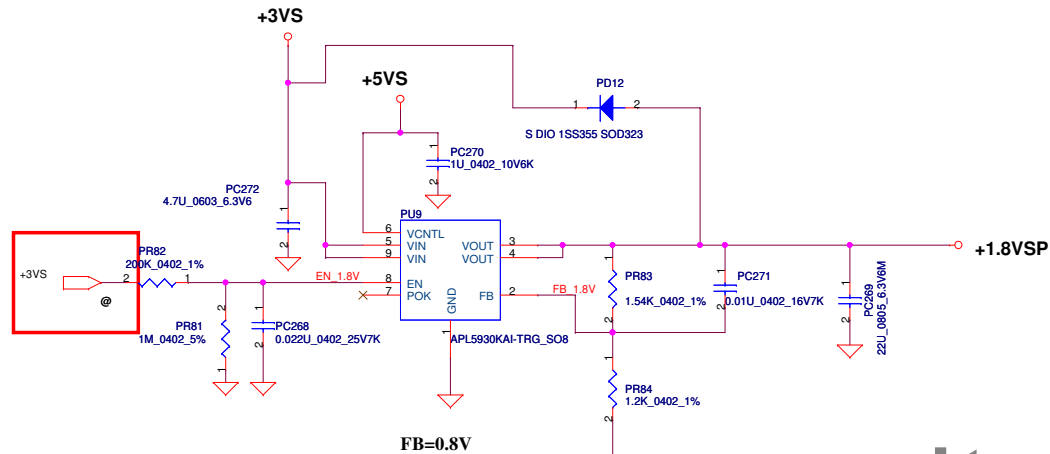


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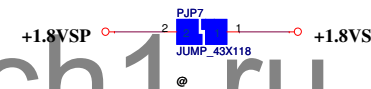
Compal Electronics, Inc.

PWR-3.3VALWP/SVALWP

Rev



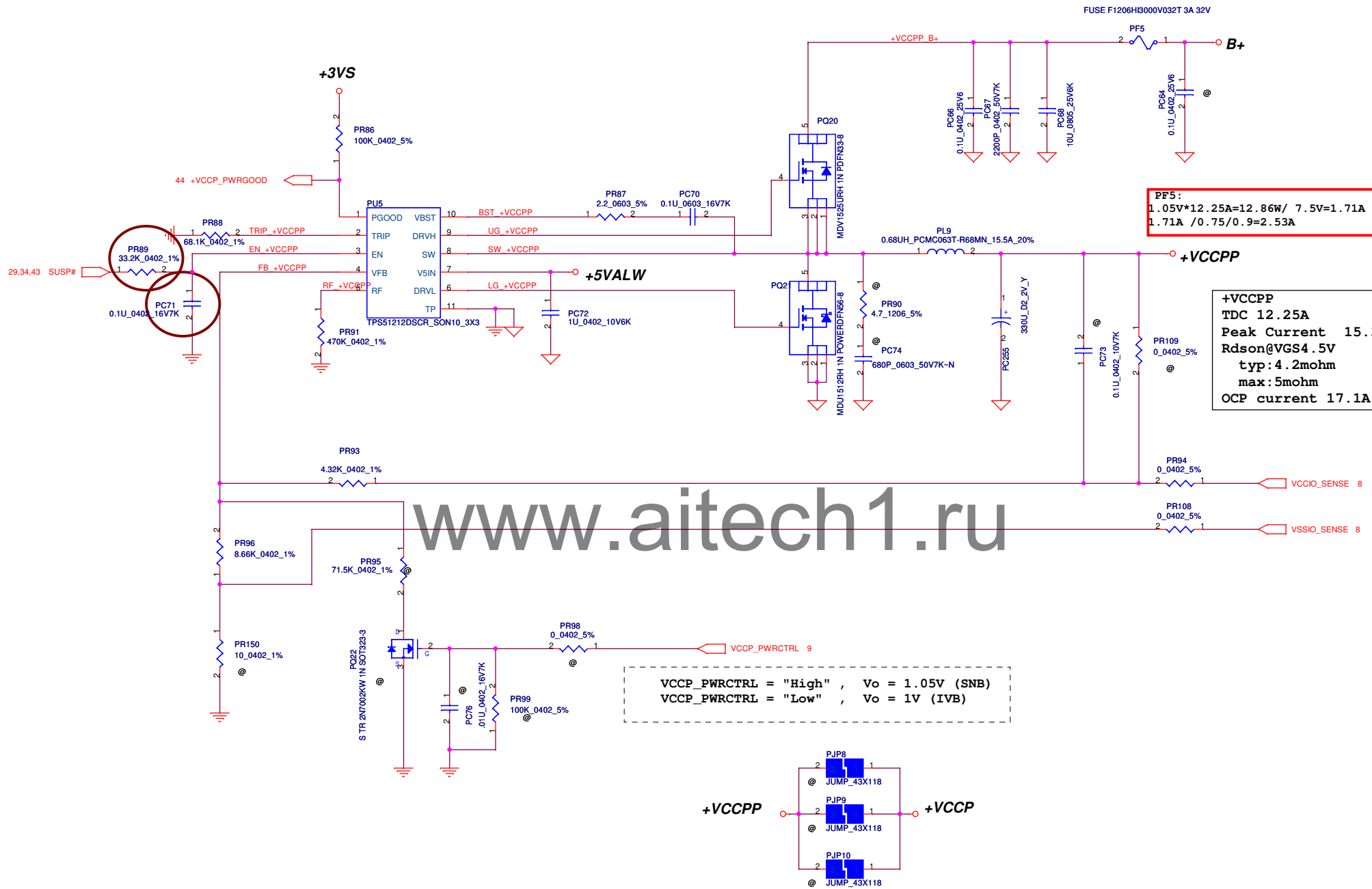
**+1.8VSP**  
**TDC = 0.99A**  
**Peak Current = 1.24A**  
**OCP = 4.7 A**



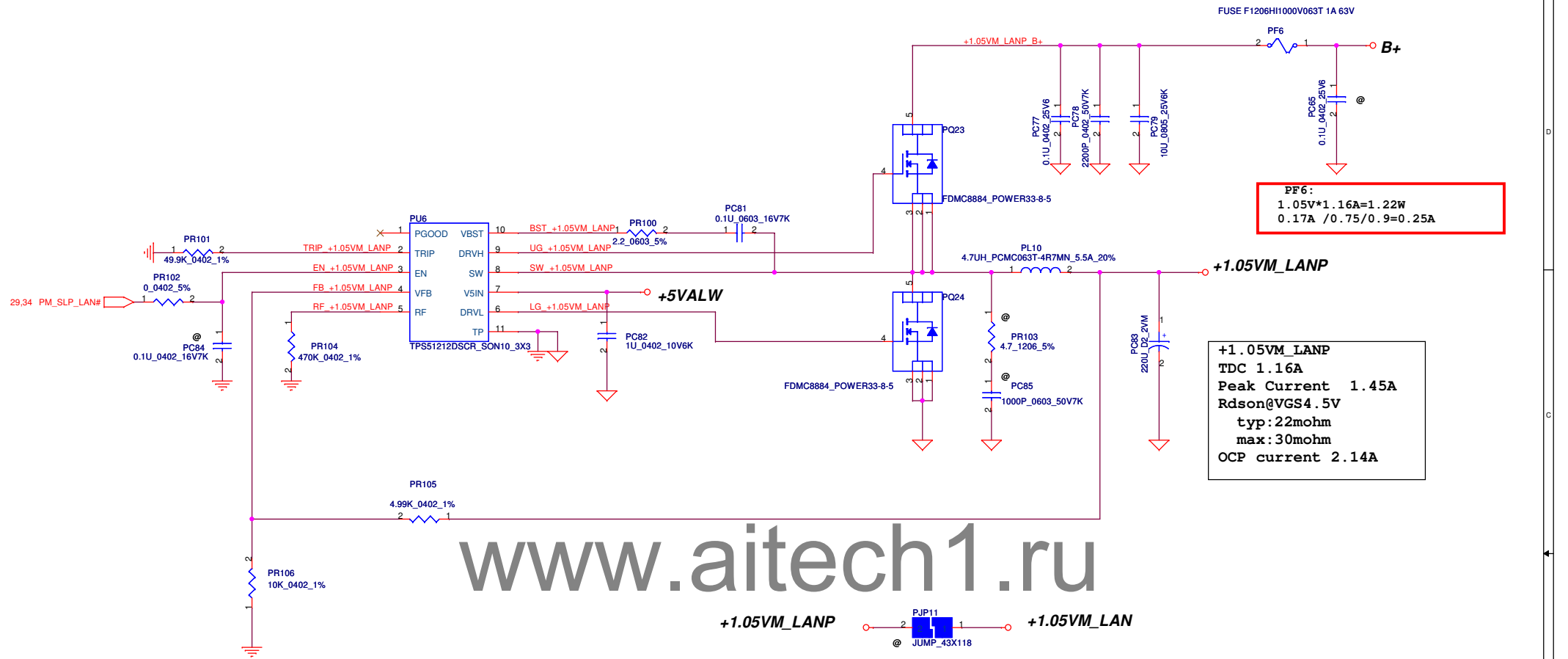
$$V_o = 0.8(1 + R_t/R_b) = 1.827V$$

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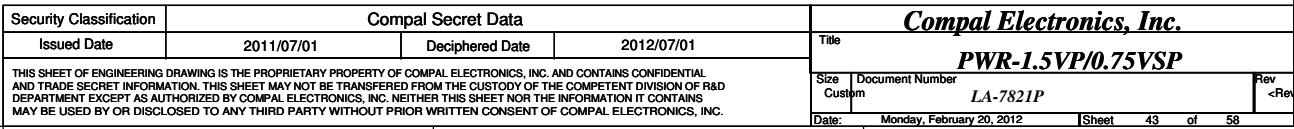
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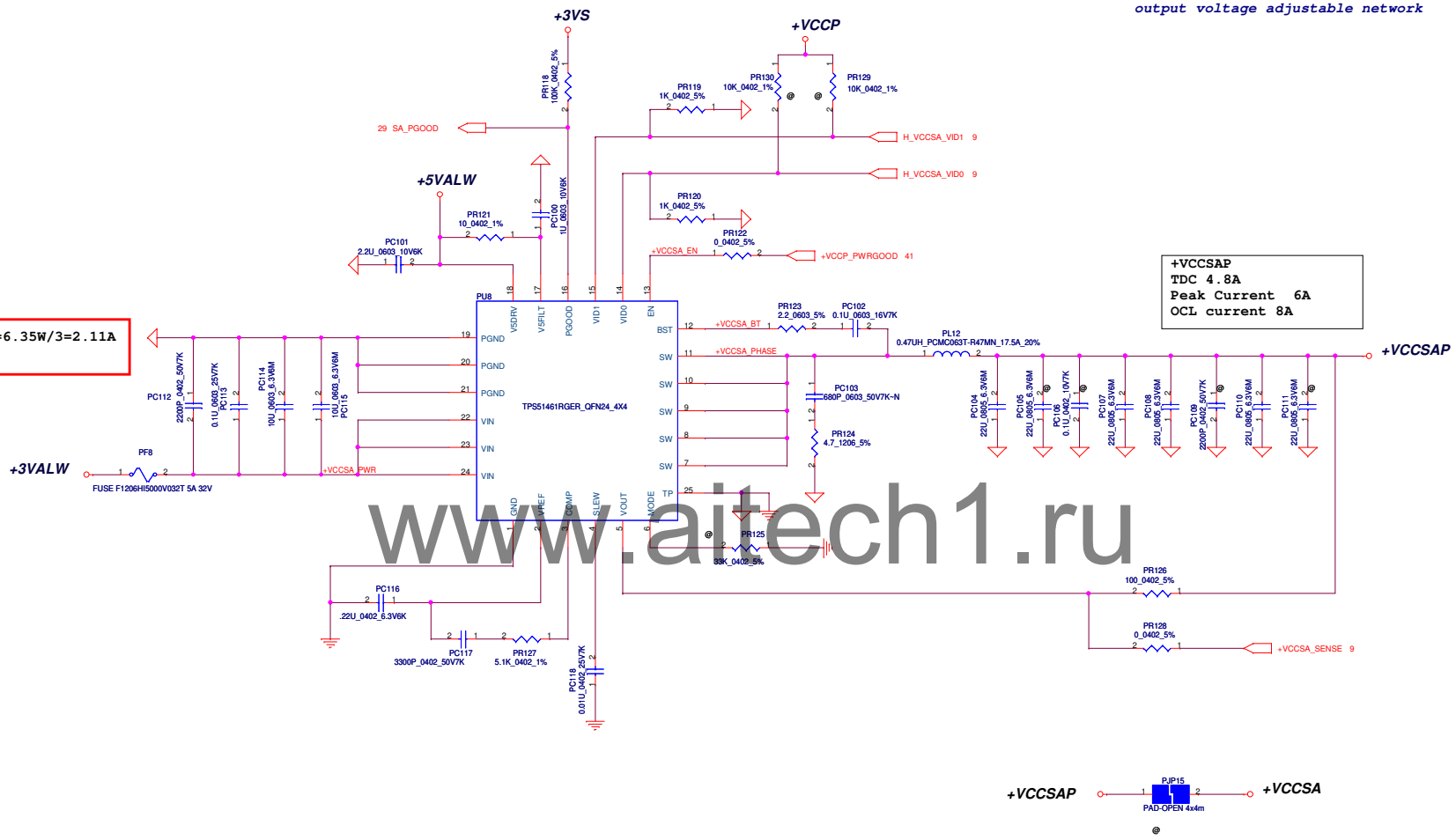
PF8: 0.9V\*6A=5.4/0.85=6.35W/3=2.11A  
2.11A/0.75/0.88=3.2A

The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCCSAP  
TDC 4.8A  
Peak Current 6A  
OCL current 8A

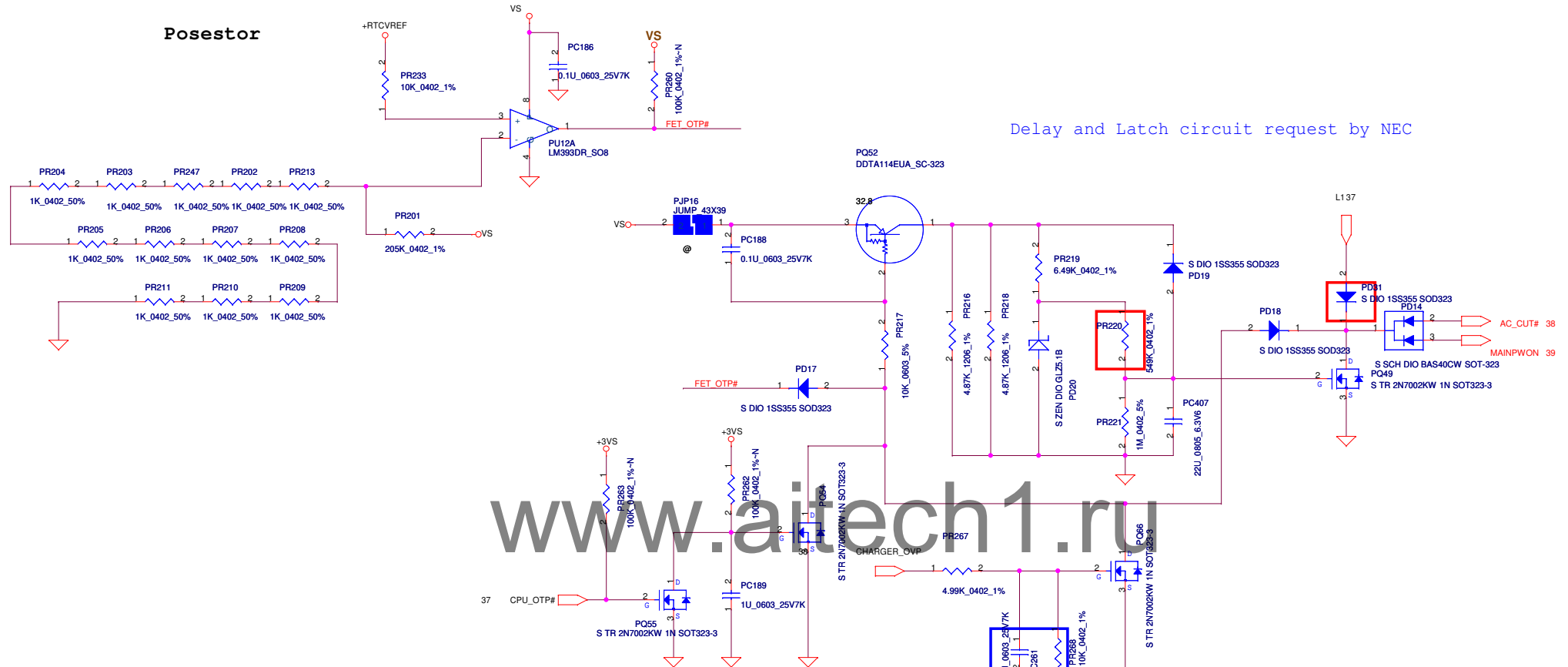


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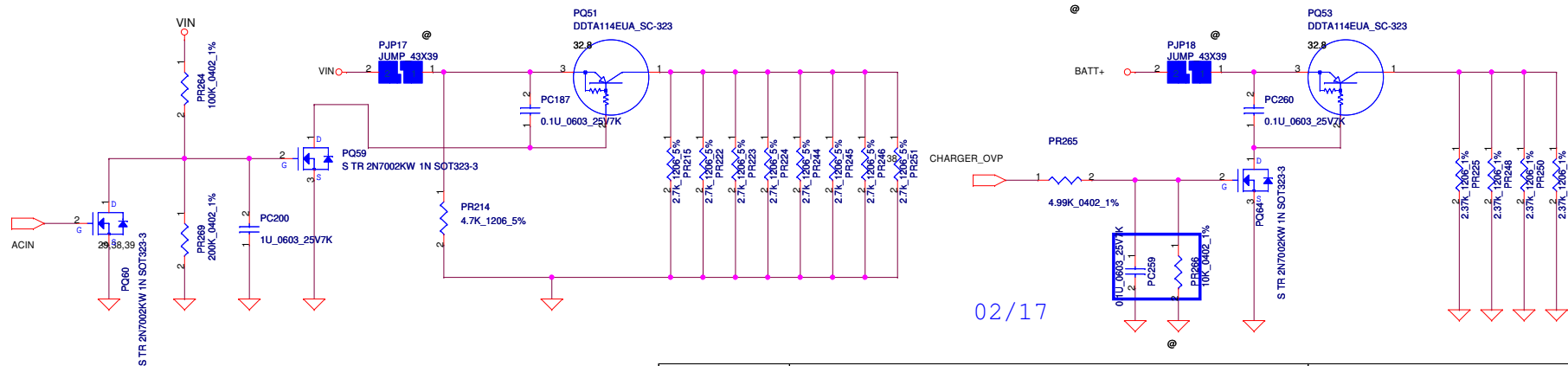




## Posestor

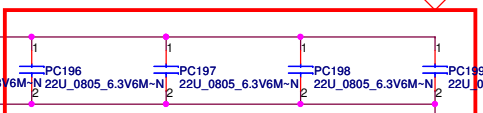


Remaining voltage discharge circuit request by NEC

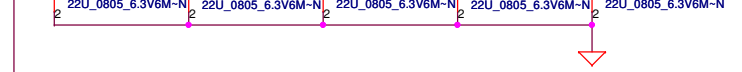
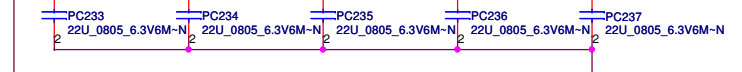
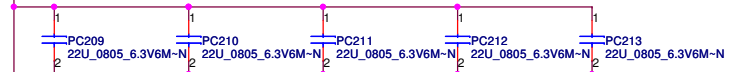


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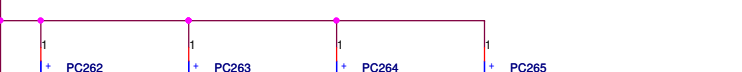
# **+VCC\_CORE**



# **+VCC\_CORE**

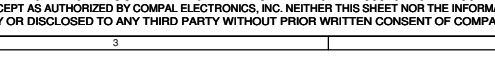
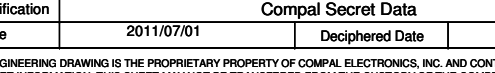
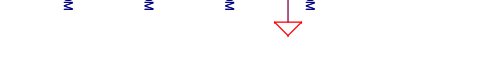
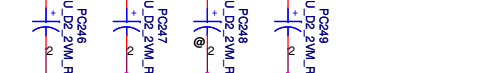
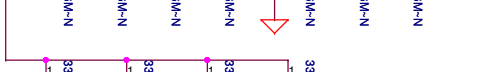
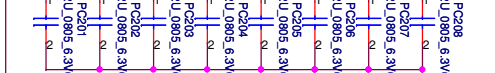


# **+VCC\_CORE**



# **+VCC\_CORE**

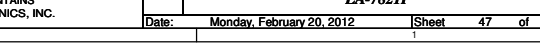
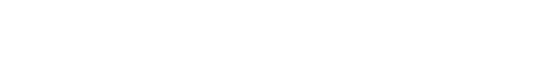
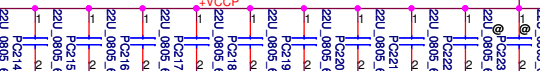
# **+VCC\_GFXCORE\_AXG**



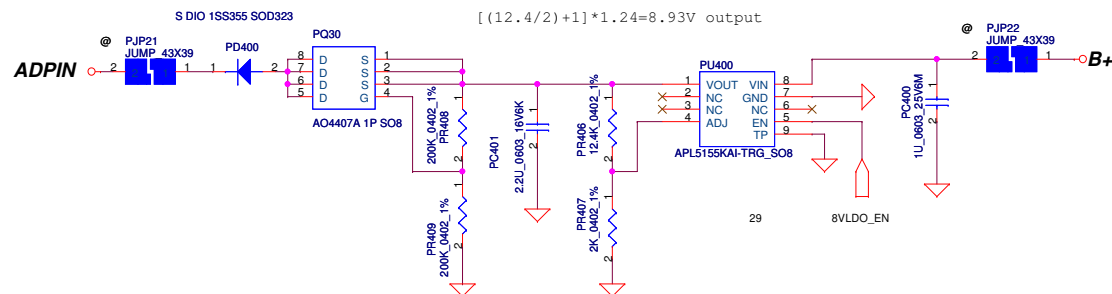
Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

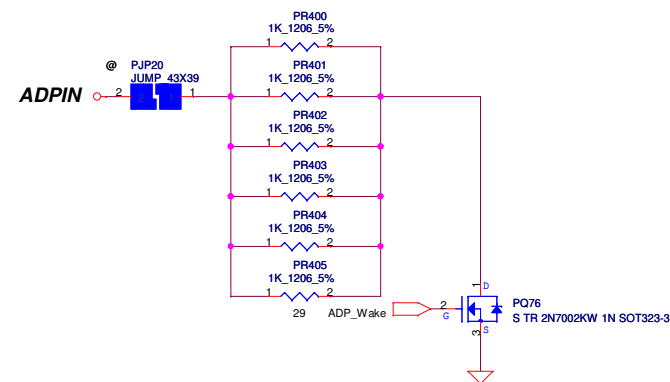
# **+VCCP**



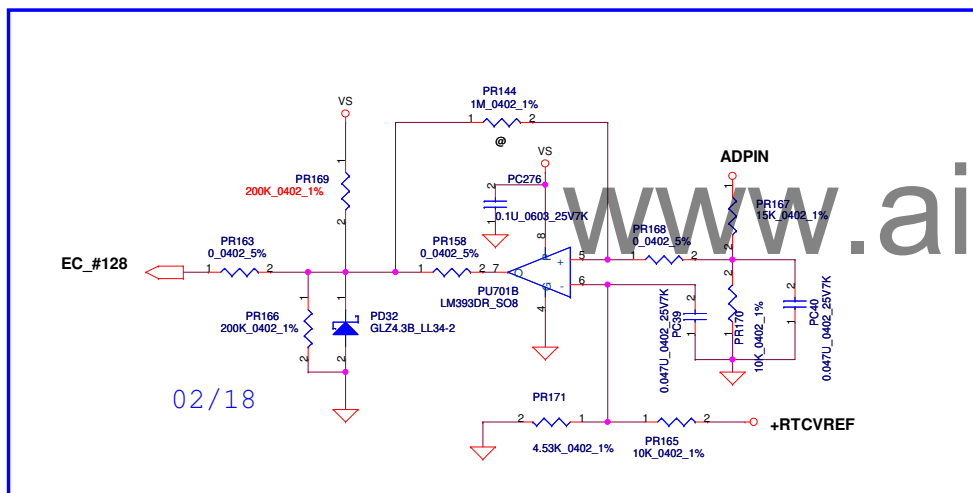
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System power on, ADP\_OFF must keep Low  
0 W ADP enable, when system complete S4 S5, ADP\_OFF keep high



When ADP will wake up from standby mode, ADP\_Wake keep high,  
it will increase system load.



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37 48	PWR_DCIN / BATT CONN / OTP PWR_OW ADP	11' 09/02	Compal_Roger	ADD 0 W adapter circuit	ADD SB502060000 PQ77 PQ78,SD034200380 PR135 PR151 ADD SD034150380 PR156, Reserve SD028000080 PR152 and PJP19 ADD SC1SS355010 PD400, SE132225KN0 PC401, SA000057Q00 PU400 ADD SD034110280 PR406, SD034200180 PR407, SE000009RN0 PC400 ADD SD001100180 PR400 PR401 PR402 PR403 PR404 PR405 ADD SB502060000 PQ76	0.1
2	38	PWR_CHARGER_BQ24737	11' 09/02	Compal_Roger	Change Charger IC solution for Hybrid power	PU2 from ISL87331C to BQ24737	0.1
3	38	PWR_CHARGER_BQ24737	11' 11/09	Compal_Toby	base on ES2 issue liat item1, NECP already implement 1 atch function, so no need this circuit.	Remove PQ65, PR115, PC97, PR114, PR144, PD23, PR136, PR138, PQ35, PQ36	0.2
4	45	P45-PWR-CPU_CORE	11' 11/09	Compal_Toby	U3CR change the mosfet solution from package 3x3 to 5x6 to improve material thermal.	Remove PQ34 ,PQ30 ,PQ42 Change MDV1525 to AON6514,Location:PQ33, PQ29, PQ41	0.2
5	46	P46-PWR-Posestor	11' 11/09	Compal_Toby	ADD the diode to avoid B+ is unstable When AC_CUT# is low.	ADD PD31 (1SS355)	0.2
6	46	P46-PWR-Posestor	11' 11/09	Compal_Toby	base on ES2 issue list item 13, change the valu to meet the spec.	Chnage 619K to 549K. Location:PR220	0.2
7	45	P45-PWR-CPU_CORE	11' 11/09	Compal_Toby	ADD JUMP for test.	ADD PJP20, PJP21	0.2
8	43	1.5VP	11' 11/10	Compal_Aaron	for deadtime	change PQ26 form MDU1512 to AON6508	
9	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust vcore LL	change PR749 form 2.15k to 2.1k	
10	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust vcore OCP	change PR753 form 475 to 499	
11	47	PROCESSOR DECOUPLING	11' 11/10	Compal_Aaron	for AXG ripple	ADD PC230, PC273, PC274	
12	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust AXG Ringback	pop PR712 and PC711	
13	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust AXG dynamic	change PC701 form 330p to 820p	
14	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust AXG dynamic	change PR701 form 2k to 2.49k	
15	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust AXG LL	change PR702 form 2.55k to 2.49k	
16	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust AXG OCP	change PR713 form 634 to 348	
17	45	CPU_CORE	11' 11/10	Compal_Aaron	adjust AXG transient	pop Pc710	
18	48	OW ADP	11' 11/11	Compal_Aaron	for DC IN reverse protection	add PQ30, PR408, PR409	

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
19	38	CHARGER BQ24737	11' 11/11	Compal_Aaron	adjust BATT OVP	change PR153 form 698k to 402k	0.1
20	42	1.05VM_LANP	11' 11/11	Compal_Aaron	adjust 1.05VM OCP	change PQ24 form FDMC7692S to FDMC8884	
21	42	1.05VM_LANP	11' 11/11	Compal_Aaron	adjust 1.05VM OCP	change PR101 form 20k to 49.9k	0.1
22	38	CHARGER BQ24737	11' 11/14	Compal_Aaron	no function	depop PR327	0.2
23	40	1.8VSP	11' 11/14	Compal_Aaron	for power sequence	change PR82 form 10k to 200k	0.2
24	48	0W ADP	11' 11/14	Compal_Aaron	adjust 0W ADP voltage	change PR406 form 11k to 12.4k	0.2
25	48	0W ADP	11' 11/14	Compal_Aaron	for power consumption	change PR408 form 10k to 200k	0.2
26	48	0W ADP	11' 11/14	Compal_Aaron	for power consumption	change PR409 form 10k to 200k	0.2
27	38	CHARGER BQ24737	11' 11/15	Compal_Aaron	adjust charger OVP	change PR145 form 178k to 165k	
28	38	CHARGER BQ24737	11' 11/15	Compal_Aaron	adjust charger OVP	change PR145 form 165k to 187k	
29	38	CHARGER BQ24737	11' 11/15	Compal_Aaron	adjust charger OVP	change PR143 form 33.2k to 0	
30	38	CHARGER BQ24737	11' 11/15	Compal_Aaron	adjust charger OVP	depop PR140	
31	48	0W ADP	11' 11/25	Compal_Aaron	for VX model	pop PC400, PC401,PD400,PQ11,PQ30,PQ76,PQ77, PQ78, PR135,PR151, PR156,PR272,PU400,PR400,PR401,PR402,PR403,PR404,PR405,PR406, PR407,PR408,PR409	
32	43	1.5VP	11' 12/20	Compal_Aaron	for dynamic output	depop PR97	
33	43	1.5VP	11' 12/20	Compal_Aaron	for dynamic output	pop PR270 / PR271	
34	43	3VALWP / 5VALWP	11' 12/20	Compal_Aaron	for KB9012	change PR76 from 10k to 2.2k	
35	46	Prosestor	11' 12/20	Compal_Aaron	reverse PD19	reverse PD19	
36	38	CHARGER BQ24737	11' 12/20	Compal_Aaron	combine OP	combine PU701 to PU12B	
37	41	VCCPP	11' 12/20	Compal_Aaron	for power sequency	pop PC71	

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## Version Change List (P. I. R. List)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
38	41	VCCPP	11' 12/20	Compal_Aaron	for power sequency	change PR89 from 0ohm to 33.2kohm	
39	40	1.8VSP	11' 12/22	Compal_Aaron	LDO EN internally	depop PR82	
40	40	1.8VSP	11' 12/22	Compal_Aaron	LDO EN internally	change PR81 from 4.7k to 1M ohm	
41	40	1.8VSP	11' 12/22	Compal_Aaron	LDO EN internally	change PC268 form0.1u to 0.022uF	
42	37	DCIN / BATT CONN / OTP	11' 12/22	Compal_Aaron	for RTC battery	remove PR36, PR37	
43	46	Prosestor	11' 12/22	Compal_Aaron	combine OP	combine PU701 to PU12B	
44	41	VCCPP	11' 12/23	Compal_Aaron	for output voltage	change PR93 from 4.99k to 4.32k	
45	38	CHARGER BQ24737	11' 12/23	Compal_Aaron	for charge current 3.85A	change PF3 from 5A to 6A	
46	48	OW ADP	11' 12/26	Compal_Aaron	add jumper	add PJP22	
47	45	CPU / AXG	11' 12/26	Compal_Aaron	increase input cap capacitance	change PC722 from 100uF to 220uF	
48	45	CPU / AXG	11' 12/26	Compal_Aaron	form AXG OCP	change PR713 from 348 to 383 ohm	
49	45	CPU / AXG	11' 12/26	Compal_Aaron	form AXG LL	change PR702 from 2.49k to 2.87k ohm	
50	45	CPU / AXG	11' 12/26	Compal_Aaron	form Vcore OCP	change PR753 from 499 to 453 ohm	
51	45	CPU / AXG	11' 12/26	Compal_Aaron	form Vcore transient	change PC745 from 22nF to 47nF	
52	45	CPU / AXG	11' 12/26	Compal_Aaron	form Vcore transient	PC747 pop	
53	47	PROCESSOR DECOUPLING	11' 12/26	Compal_Aaron	form Vcore ocp	PC265 pop	
54	46	Prosestor	11' 12/27	Compal_Aaron	for protection circuit	change PR219 from 10k to 6.49k	
55	37	DCIN / BATT CONN / OTP	12' 01/02	Compal_Aaron	for ADP protection 75W(VX)	add PR5 4.32k	
56	45	CPU / AXG	12' 01/09	Compal_Aaron	form Vcore transient	change HS MOS PQ29, PQ33, PQ41 form AON6514 to AON6428L	

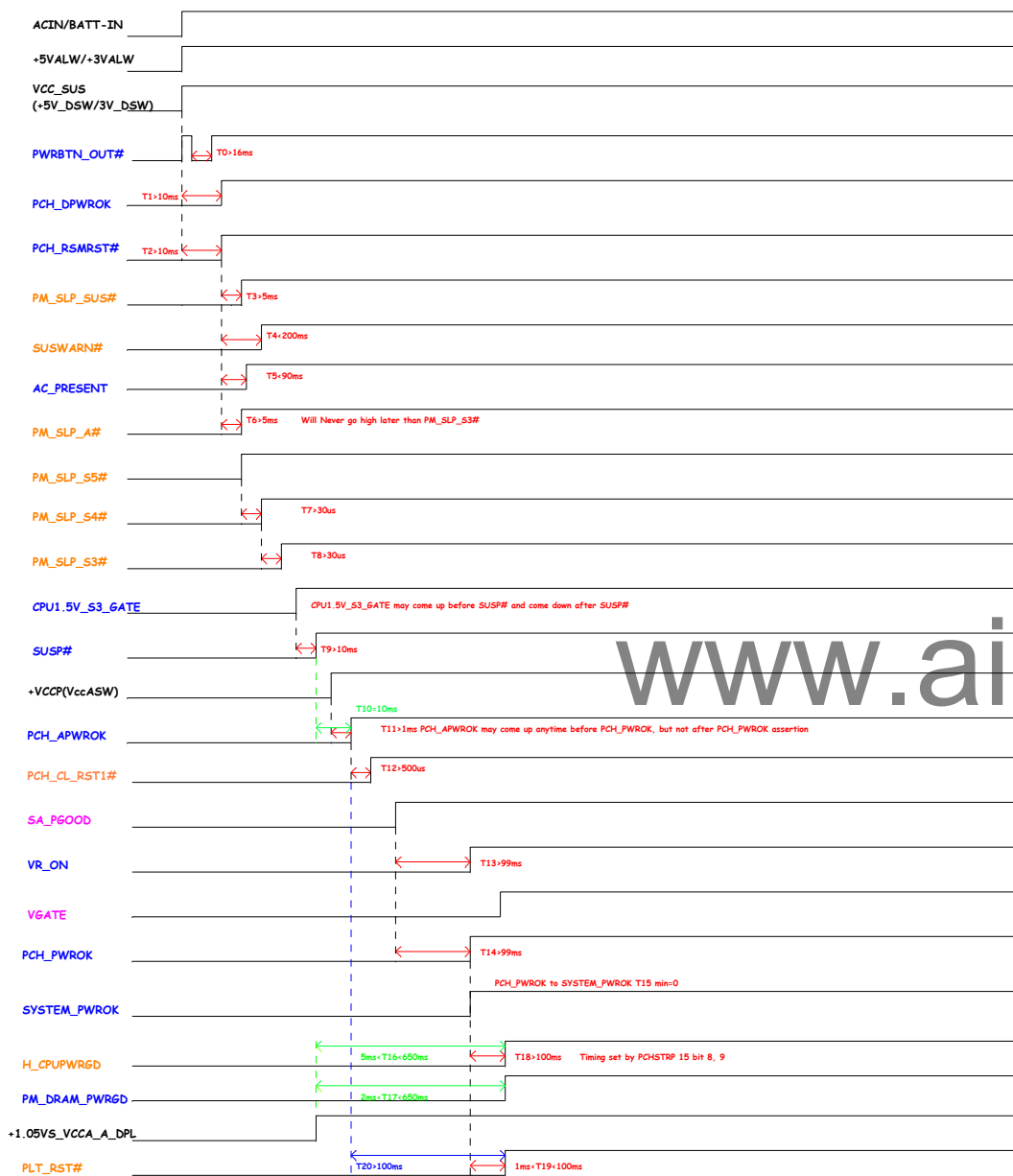
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57	39	3VALWP/5VALWP	12' 02/14	Compal_Aaron	for FUSE derating	change PF4 from 5A to 6A	
58	37	DCIN / BATT CONN / OTP	12' 02/14	Compal_Aaron	for FUSE derating	change PF2 from 12A to 15A	
59	43	1.5VP	12' 02/14	Compal_Aaron	for FUSE derating	change PF7 from 3A to 5A	
60	45	CPU / AXG	12' 02/14	Compal_Aaron	for FUSE derating	change PF9 from 8A to 10A	
61	45	CPU / AXG	12' 02/14	Compal_Aaron	for FUSE derating	change PF12 from 6A to 8A	
62	45	CPU / AXG	12' 02/14	Compal_Aaron	for AXG transient	change PC705 from 47pF to 33pF	
63	45	CPU / AXG	12' 02/14	Compal_Aaron	for AXG transient	change PC710 from 68nF to 0.1uF	
64	45	CPU / AXG	12' 02/14	Compal_Aaron	for Vcore transient	depop PC745	
65	45	CPU / AXG	12' 02/14	Compal_Aaron	for Vcore transient	mount PR763 and PC751	
66	47	PROCESSOR DECOUPLING	12' 02/14	Compal_Aaron	for Vcore transient	change PC196, PC197, PC198, PC199 from 10uF to 22uF	
67	46	Posestor	12' 02/17	Compal_Aaron	for power consumption	unmount PR268, PR266, PD28	
68	46	Posestor	12' 02/17	Compal_Aaron	for power consumption	change PC261, PR259 from 1uF to 0.1uF	
69	37	DCIN / BATT CONN / OTP	12' 02/17	Compal_Aaron	for power consumption	change PR141, PR142 from 10K ohm to 200k ohm	
70	48	0W ADP	12' 02/18	Compal_Aaron	for detect 0W ADP	add PU701B relate resistor and capacitor	
71				Compal_Aaron			
72				Compal_Aaron			
73				Compal_Aaron			
				Compal_Aaron			
				Compal_Aaron			

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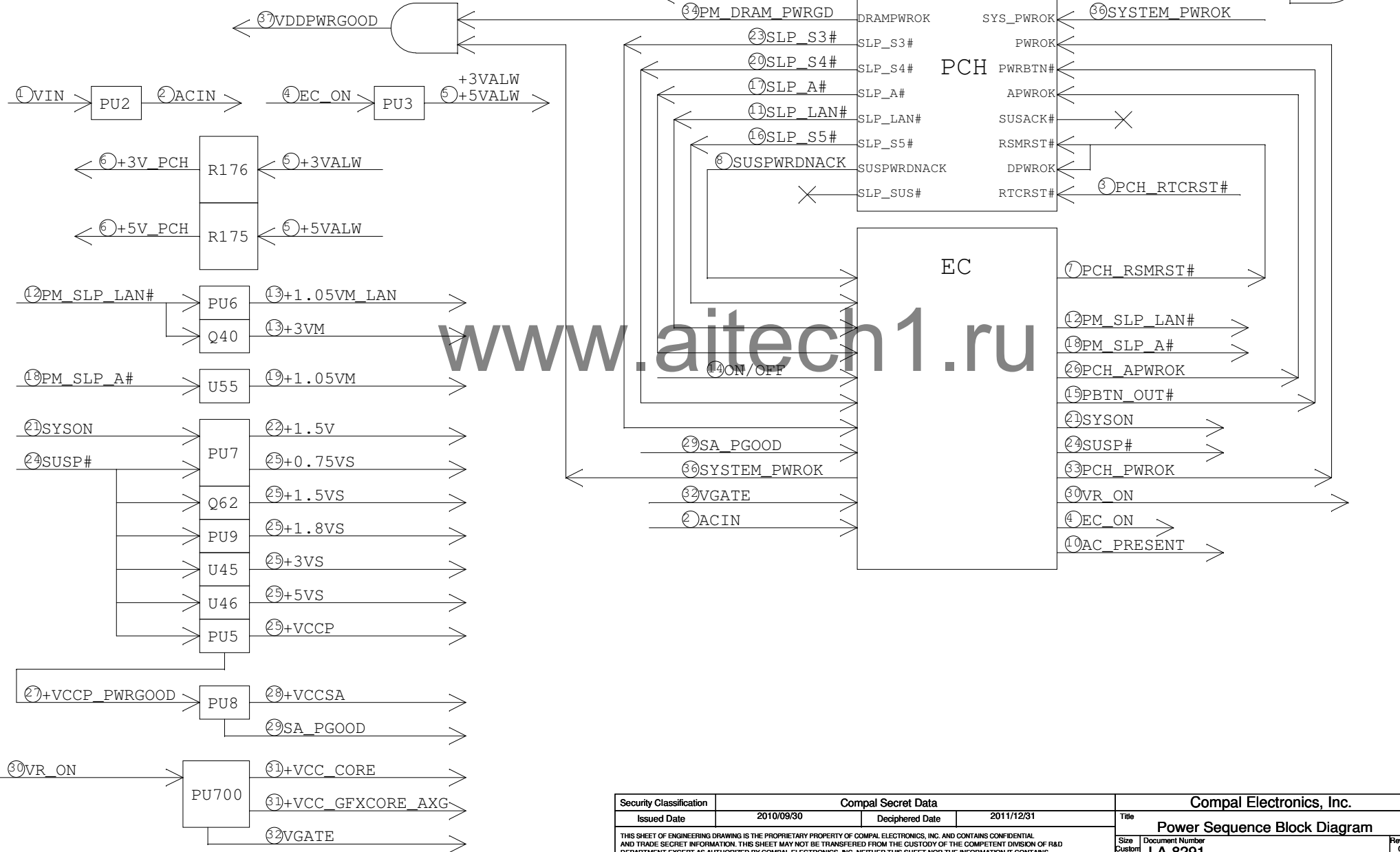
# Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

# COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*  
PCB NAME: *LA-8291*  
REVISION:  
DATE: *2011/09/014*



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.02	PG#12	correct remark typo.	8/22	PRE-ES1
2		HW Design	0.02	PG#12	Add BBS table.	8/22	PRE-ES1
3		HW Design	0.02	PG#15	Add test point T207, T208 and T209.	8/22	PRE-ES1
4		Panther Point EDS	0.02	PG#17	This pin can be left as no connect.	8/22	PRE-ES1
5		Panther Point EDS	0.02	PG#17	This pin can be left as no connect.	8/22	PRE-ES1
6		Panther Point EDS	0.02	PG#18	This pin can be left as no connect.	8/22	PRE-ES1
7		Panther Point EDS	0.02	PG#18	This pin can be left as no connect.	8/22	PRE-ES1
8		Panther Point EDS	0.02	PG#18	This pin can be left as no connect.	8/22	PRE-ES1
9		HW Design	0.02	PG#34	Delete +1.05VS power transfer circuit.	8/22	PRE-ES1
10		HW Design	0.02	PG#17	Change +1.05VS to VCCP.	8/22	PRE-ES1
11		HW Design	0.02	PG#18	Change +1.05VS to VCCP.	8/22	PRE-ES1
12		HW Design	0.02	PG#13	Add remard of SMBus device address.	8/22	PRE-ES1
13		HW Design	0.02	PG#21	Change currenct limit circuit.	8/22	PRE-ES1
14		HW Design	0.02	PG#16	Change RH169 as un-monted.	8/22	PRE-ES1
15		HW Design	0.02	PG#16	Change net STP_PCI# to PCH_GPIO34.	8/22	PRE-ES1
16		HW Design	0.02	PG#12	Delete CABCP function.	8/22	PRE-ES1
17		HW Design	0.02	PG#20	Change currenct limit circuit.	8/22	PRE-ES1
18		HW Design	0.02	PG#25	Delete net EC MUTE#.	8/22	PRE-ES1
19		HW Design	0.02	PG#13	Delete ITPXDR clock.	8/22	PRE-ES1
20		HW Design	0.02	PG#18	Delete DcpSus circuit.	8/22	PRE-ES1
21		HW Design	0.02	PG#14	Change RH113 to a 0ohm resistor.	8/22	PRE-ES1
22		HW Design	0.02	PG#18	Change RH201 to a 0ohm resistor.	8/22	PRE-ES1
23		HW Design	0.02	PG#12	Change net PCH_SPI_CLK to PCH_SPI_CLK_R.	8/22	PRE-ES1
24		HW Design	0.02	PG#34	Change net +1.05VS to +VCCP	8/22	PRE-ES1
25		HW Design	0.02	PG#29	Change net SW_CONFIG1 to pin 83	8/22	PRE-ES1
26		HW Design	0.02	PG#32	Pin swap for layout request.	8/22	PRE-ES1
27		HW Design	0.02	PG#12	Change BOM structure.	8/22	PRE-ES1
28		HW Design	0.02	PG#29	Change BOM structure.	8/25	PRE-ES1
29		HW Design	0.02	PG#32	Pin swap for layout request.	8/25	PRE-ES1
30		HW Design	0.02	PG#34	Delete Q46.	8/25	PRE-ES1
31		HW Design	0.02	PG#12	Change PCH BOM structure.	8/25	PRE-ES1
32		HW Design	0.02	PG#29	Delete EC function CHG_OVP.	8/25	PRE-ES1
33		HW Design	0.02	PG#16	Change signal direction	8/26	PRE-ES1
34		HW Design	0.02	PG#29	Add 0W ADP design.	8/26	PRE-ES1
35		HW Design	0.02	PG#28	Change SATA re-driver IC for Gen3.	8/26	PRE-ES1

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36		NECP recommend	0.02	PG#15	Change OC7# to OC6# for port 12 and 13 use.	8/27	PRE-ES1
37		NECP recommend	0.02	PG#14	Change RH135 as no-stuff.	8/27	PRE-ES1
38		NECP recommend	0.02	PG#12	Pull-up to +3V_PCH.	8/27	PRE-ES1
39		HW Design	0.02	PG#12	Add ROM 2 for new BOM structure.	8/27	PRE-ES1
40		HW Design	0.02	PG#21	Change RV1531 as stuff for vendor request.	8/27	PRE-ES1
41		NECP recommend	0.02	PG#15	Change Felica to USB port 10.	8/27	PRE-ES1
42		NECP recommend	0.02	PG#11	Delete net M_THERMAL#.	8/27	PRE-ES1
43		NECP recommend	0.02	PG#27	Add LPC to JMINI1.	8/27	PRE-ES1
44		NECP recommend	0.02	PG#27	Delete +1.5VS for JMINI2 and JMINI3.	8/27	PRE-ES1
45		HW Design	0.02	PG#27	Delete +1.5VS for JMINI1.	8/27	PRE-ES1
46		NECP recommend	0.02	PG#17	Update PCH power rail table.	8/27	PRE-ES1
47		HW Design	0.02	PG#34	Change U55 to AO4478L.	8/27	PRE-ES1
48		NECP recommend	0.02	PG#5	Delete RC67 and RC20.	8/27	PRE-ES1
49		HW Design	0.02	PG#32	Modify USB 3.0 schematic.	8/31	PRE-ES1
50		NECP recommend	0.03	PG#27	Delete JMINI3.	9/1	PRE-ES1
51		NECP recommend	0.03	PG#9	Modify current comment.	9/1	PRE-ES1
52		NECP recommend	0.03	PG#32	Add de-coupling capacitor.	9/1	PRE-ES1
53		HW Design	0.03	PG#25	Change connector for mechanical request.	9/1	PRE-ES1
54		NECP recommend	0.03	PG#9	Enable M3 circuit.	9/1	PRE-ES1
55		HW Design	0.03	PG#29	Change net name from ME_Flash to ME_EN.	9/2	PRE-ES1
56		HW Design	0.03	PG#12	Change resistor from 15 ohm to 33 ohm.	9/2	PRE-ES1
57		HW Design	0.03	PG#29	Delete C130.	9/5	PRE-ES1
58		HW Design	0.03	PG#25	Change audio to ALC-269-VC	9/5	PRE-ES1
59		HW Design	0.03	PG#14	Change net from PCH_APWROK_R to APWROK.	9/6	PRE-ES1
60		HW Design	0.03	PG#14	Change net from SYSTEM_PWROK_R to SYS_PWROK.	9/6	PRE-ES1
61		NECP recommend	0.03	PG#29	Change R502 as non-stuff.	9/7	PRE-ES1
62		HW Design	0.03	PG#12	Add RH274.	9/7	PRE-ES1
63		NECP recommend	0.03	PG#5	Change +3VALW to +3V_PCH.	9/7	PRE-ES1
64		HW Design	0.03	PG#32	Swap for layout request.	9/7	PRE-ES1
65		NECP recommend	0.03	PG#28	Add CS992.	9/7	PRE-ES1
66		NECP recommend	0.03	PG#9	Change RC55 and RC71 as non-stuff.	9/7	PRE-ES1
67		HW Design	0.03	PG#18	Delete T210 for layout request.	9/7	PRE-ES1
68		HW Design	0.03	PG#15	Delete T207, T208 and T209 for layout request.	9/7	PRE-ES1
69		HW Design	0.03	PG#12	Change VCC power of ROM_2 from +3VS to +3V_PCH.	9/7	PRE-ES1
70		HW Design	0.04	PG#30	Change Conn value to meet Conn List Table.	9/9	PRE-ES1

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
71		NECP recommend	0.05	PG#25	Connect to GND	9/13	PRE-ES1
72		NECP recommend	0.05	PG#25	Change resistors from 75 ohm to 59 ohm.	9/13	PRE-ES1
73		NECP recommend	0.05	PG#29	Change resistors from 2.2K ohm to 4.7K ohm.	9/13	PRE-ES1
74		NECP recommend	0.05	PG#17	Change CH50 as mounted.	9/13	PRE-ES1
75		NECP recommend	0.05	PG#24	Change RL165 and R167 as mounted.	9/13	PRE-ES1
76		HW Design	0.06	PG#34	Change BOM structure.	9/14	PRE-ES1
77		HW Design	0.06	PG#29	Re-assign GPIO for EC team request.	9/14	PRE-ES1
78		NECP recommend	0.06	PG#28	Reserve R109 for NECP request.	9/14	PRE-ES1
79		HW Design	0.07	PG#29	Delete X1.	9/15	PRE-ES1
80		NECP recommend	0.07	PG#23	add layout comment.	9/15	PRE-ES1
81		HW Design	0.07	PG#12	Reserve EMC solution.	9/15	PRE-ES1
82		HW Design	0.07	PG#29	Change power plane for 0W adapter.	9/15	PRE-ES1
83		HW Design	0.08	PG#14	Change BOM structure.	9/16	PRE-ES1
84		HW Design	0.08	PG#9	Add SMT comment.	9/16	PRE-ES1
85		HW Design	0.08	PG#29	Re-assign GPIO for EC team request.	9/16	PRE-ES1
86		HW Design	0.10	PG#29	Change ACIN detect circuit.	9/22	PRE-ES2
87		HW Design	0.10	PG#28	Swap single.	9/29	PRE-ES2
88		HW Design	0.10	PG#12	Change RH273 as non-mount.	10/3	PRE-ES2
89		HW Design	0.10	PG#29	Change SW_CONFIG1 detection circuit.	10/24	PRE-ES2
90		HW Design	0.10	PG#34	R957, Q47A and R1013 are not necessary for VX.	10/24	PRE-ES2
91		HW Design	0.10	PG#33	Change power rail from +3VALW to +3VLP for LID.	10/24	PRE-ES2
92		HW Design	0.10	ALL	Change material to fix shortage issue. Q40, Q89. from SB934130000 to SB000006R10. Q36, 41, 42, 43, 45, 49, 50, 53, 58, 100, 111 and QV84. from SB000009610 to SB000009620. Change QE8 from SB570020110 to SB000009620.	10/31	PRE-ES2
93		HW Design	0.10	PG#29	Re-assign EC pin: GPIO17: EC_TX_P80_CKL GPXIOA07: SLP_LAN# GPIO5D: VGATE	10/31	PRE-ES2
94		HW Design	0.10	PG#24	Change YH2 and YL5 from SJ100009B00 to SJ10000B700.	10/31	PRE-ES2
95		HW Design	0.10	ALL	Delete 930 co-lay circuit.	10/31	PRE-ES2
96		HW Design	0.10	PG#12	Change from 33 ohm to 47 ohm.	11/2	PRE-ES2
97		HW Design	0.10	PG#24	Change PLT_RST#_LAN circuit.	11/4	PRE-ES2
98		HW Design	0.10	PG#32	Add USB co-lay circuit.	11/4	PRE-ES2
99		HW Design	0.10	PG#12	Change SPI ROM structure.	11/4	PRE-ES2
100		HW Design	0.10	PG#26	Change PLT_RST# circuit.	11/8	PRE-ES2
101		HW Design	0.10	PG#34	Add reserve circuit C818 and C819 for timing fine-tune.	11/8	PRE-ES2
102		HW Design	0.10	PG#34	Change masterial for Q28 and Q205.	11/9	PRE-ES2
103		HW Design	0.10	PG#29	Change board ID.	11/9	PRE-ES2

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
104		HW Design	0.11	PG#33	Add D88 for ESD request.	11/11	PRE-ES2
105		HW Design	0.11	PG#29	Add R494 for reserve circuit.	11/14	PRE-ES2
106		HW Design	0.20	PG#29	Reserve C123 for PECI.	12/12	PP
107		HW Design	0.20	PG#29	Add R497 for power sequence.	12/13	PP
108		HW Design	0.20	PG#30	Add RE98 to fix LED blink issue.	12/15	PP
109		HW Design	0.20	PG#29	Change R108 to 6.8K to modify board ID.	12/15	PP
110		HW Design	0.20	PG#30	Change body diode direction of QH9.	12/15	PP
111		HW Design	0.20	PG#28	Add SATA re-driver co-lay circuit.	12/16	PP
112		HW Design	0.20	PG#5	Change RC12, RC18 and RC4 to 10K ohm.	12/19	PP
113		HW Design	0.20	PG#31	Add FU6.	12/19	PP
114		HW Design	0.20	PG#22	Change cardbus IC.	12/21	PP
115		NECP recommend	0.20	PG#22	Connect unused pins of 1394 to GND.	12/22	PP
116		HW Design	0.20	PG#29	Change D80 for ESD request.	12/26	PP
117		HW Design	0.20	PG#33	Add R101.	12/27	PP
118		HW Design	0.20	PG#12	Change CH3 to 12pF.	01/04	PP
119		HW Design	0.20	PG#23	Change C708 from SE0000069N0 to SE080105KN0.	01/04	PP
120		HW Design	0.30	PG#22	Correct part name of U27.	02/06	MRT
121		HW Design	0.30	PG#32	Change material for C232 and U233.	02/06	MRT
122		HW Design	0.30	PG#25	Change material for UA90.	02/06	MRT
123		HW Design	0.30	PG#33	R101 is mounted.	02/06	MRT
124		HW Design	0.30	PG#33	Delete R1773.	02/06	MRT
125		HW Design	0.30	PG#29	Change R108 to modify board ID.	02/08	MRT
126		NECP recommend	0.30	PG#05	Change RC18, RC12 and RC4 to 200 ohm to meet PDG.	02/10	MRT
127		NECP recommend	0.30	PG#32	Change USB3.0 power rail from +3VS to +3V_PCH for fix USB device lost issue.	02/10	MRT
128		HW Design	0.30	ALL	Change 0 ohm resistors to short pattern to reduce cost.	02/13	MRT
129		HW Design	0.30	PG#33	Reserve 4 caps for ESD request.	02/20	MRT

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